06-05-00

A

Attorney Docket No.: CDST-C130-1P

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Patent Application

I hereby certify that this transmittal of the below described documents is being deposited with the United States Postal Service in an envelope bearing Express Mail Postage and an Express Mail label, with the below serial number, addressed to the Commissioner of Patents and Trademarks, Washington, D.C., 20231, on the below date of deposit.			
Express Mail Label No.:	EE588900291US	Name of Person Making the Deposit:	ANTHONY CHOU
Date of Deposit:	05/31/00	Signature of the Person Making the Deposit	Anthony Chou

Inventor(s): Jueng Gil Lee, Christopher J. Spindt, Johan Knall, Matthew A. Bonn and Kishore K. Chakravorty

Group Art Unit:

Filed: 05/31/00

Examiner:

Title: MULTILAYER ELECTRODE STRUCTURE AND METHOD FOR FORMING MULTILAYER ELECTRODE STRUCTURE FOR A FLAT PANEL DISPLAY DEVICE

The Commissioner of Patents and Trademarks
Washington, D.C. 20231
Sir:

Transmittal of a Continuation-in-Part Patent Application

Transmitted herewith is the above identified patent application, including:

- x Specification, claims and abstract, totaling 89 pages.
- ..... Formal drawings, totaling ..... pages.
- x Informal drawings, totaling 75 pages.
- x Copy of Petition for Extension of Time to provide copendency in the parent application.
- ..... Form 1449
- ..... Information Disclosure statement
- ..... Assignment(s)
- ..... Assignment Recordation Form (duplicate)
- x Declaration / Power of Attorney
- ..... A certified copy of priority application: .....

PRIORITY CLAIM

A. 35 U.S.C 119

The prior U.S. application(s), including any prior International Application designating the U.S., identified above, in turn itself claim(s) foreign priority(ies) as follows:

country	application no.	filed on
.....	.....	.....

The certified copy(ies) has (have)

☐ been filed on ..... in prior application .....
which was filed on .....

☐ is are attached

☐ Amend the specification by inserting, before the first line, the following sentence:

B. 35 U.S.C. 119(e)

"This application claims the benefit of U.S. Provisional Application(s) No(s).:

APPLICATION NO(S).:	FILING DATE
.....	.....

C. 35 U.S.C. 120, 121 and 365(c)

"This application is a continuation-in-part of and claims the benefit of copending application(s)

[x] application number 09/421,781 filed on 10/19/99

[ ] International Application ..... filed on .....

and which designated the U.S."

INVENTORSHIP STATEMENT

[x] This application discloses and claims additional disclosure by amendment and a new declaration /oath is being filed. With respect to the prior application, the inventor(s) in this application are

[ ] the same.

[x] the following additional inventor(s) have been added

Kishore K. Chakravorty

FEES DUE

The fees due for filing the specification pursuant to 37 C.F.R. § 1.16 and for recording of the Assignment, if any, are determined as follows:

CLAIMS					
	NO. OF CLAIMS		EXTRA CLAIMS	RATE	FEES
Basic Application Fee					$690.00
Total Claims	54	Minus 20=	34	X $18 =	$612.00
Independent Claims	6	Minus 3=	3	X $78 =	$234.00
If multiple dependent claims are presented, add $260.00					$0.00
Add Assignment Recording Fee of $40.00 If Assignment document is enclosed					$0.00
TOTAL APPLICATION FEE DUE					$1,536.00

PAYMENT OF FEES

1. The full fee due in connection with this communication is _ provided as follows:

[X] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 23-0085. A duplicate copy of this authorization is enclosed.

[X] A check in the amount of $1,536.00

[ ] Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 23-0085.

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

Respectfully submitted,

Date: 5/31/00

By: _____
John P. Wagner, Jr.
Reg. No. 35,398

Notification to Parent of CIP Application Filing
Applicant: **Lee et al.** FILED: **10/19/99**
Docket No.: **CDST-C130** S/N.: **09/421,781**
Title: ELECTRODE STRUCTURE AND METHOD FOR FORMING ELECTRODE STRUCTURE FOR A FLAT PANEL DISPLAY
Sir:
Please acknowledge receipt of the following:

- [X] Certificate of Mailing
- [X] Conditional Petition for an Extension of Time
- [X] Notification of Filing of CIP

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Attorney Docket No.: CDST-C130

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

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Date of Deposit:	05/31/00	Name of Person Making the Deposit:	KATHERINE RINALDI	Signature of the Person Making the Deposit:	Katherine Rinaldi

In re Application

Inventor(s): Jueng Gil Lee, Christopher J. Spindt, Johan Knall and Matthew A. Bonn

Application No.: 09/421,781

Filed: 10/19/99

Title: ELECTRODE STRUCTURE AND METHOD FOR FORMING ELECTRODE STRUCTURE FOR A FLAT PANEL DISPLAY

Assistant Commissioner for Patents
Washington, D.C. 20231

NOTIFICATION OF FILING OF CONTINUATION-IN-PART PATENT APPLICATION

[x] Notification is hereby being made of the filing of a continuation-in-part application for this case

[x] concurrently herewith.
[ ] on .....

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

Respectfully submitted,

Date: 5/31/00

By: _____
John P. Wagner, Jr.
Reg. No. 35,398

UNITED STATES PATENT APPLICATION

FOR

MULTILAYER ELECTRODE STRUCTURE AND METHOD FOR FORMING MULTILAYER ELECTRODE STRUCTURE FOR A FLAT PANEL DISPLAY DEVICE

Inventors:

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MULTILAYER ELECTRODE STRUCTURE AND METHOD FOR FORMING MULTILAYER ELECTRODE STRUCTURE FOR A FLAT PANEL DISPLAY DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

This Application is a Continuation-in-Part of copending United States Patent Application Serial No. 09/421,781 entitled "ELECTRODE STRUCTURE AND METHOD FOR FORMING ELECTRODE STRUCTURE FOR A FLAT PANEL DISPLAY" to Lee et al. filed October 19, 1999. This Application is also related to United States Patent Application Entitled "DUAL-LAYER METAL FOR FLAT PANEL DISPLAY", which is filed concurrent with the filing of the present Application.

FIELD OF THE INVENTION

The present claimed invention relates to the field of flat panel displays. More particularly, the present claimed invention relates to a method for forming an electrode structure for a flat panel display.

BACKGROUND ART

Display devices such as, for example, flat panel display devices typically utilize a cathode structure that is formed over a backplate. The cathode structure includes row electrodes and column electrodes that are used to activate regions of field emitters. The field emitters emit electrons that are directed towards respective pixel or sub-pixel regions on a faceplate. By selectively activating row electrodes and column electrodes, electrons are emitted that strike the respective pixel or sub-pixel regions on the faceplate. Typically, phosphors are coated on the inside of the faceplate.

The electrons strike the phosphors, producing red, green or blue visible light that forms a visible display.

In prior art processing techniques, aluminum is commonly used for forming row electrodes and column electrodes. However, aluminum is subject to hillock formation. Hillock formation results in nonuniform planarization and can cause both row and column shorts to occur.

In one recent prior art process a layer of tantalum is deposited over the aluminum layer for reducing hillock formation. However, the resulting structure has a conductivity that is too low for use in large flat panel display devices. That is, though this process is sufficient for making small flat panel displays, the resulting row or column has too high a resistivity to be used in making large flat panel displays.

In prior art processes that use a layer of aluminum that is overlain by a layer of tantalum, the layer of aluminum is first deposited by placing the backplate into a sputtering chamber. Once the aluminum layer deposition is complete, the backplate is removed from the sputtering chamber. The layer of aluminum is then masked. More particularly, photoresist is deposited over the backplate, and the photoresist is exposed. The layer of aluminum is then etched using a wet etch process to form the desired aluminum structure.

The backplate is then placed into a second sputtering chamber that deposits the tantalum layer. Once the deposition of the tantalum layer is complete, the backplate is removed from the second sputtering chamber.

The layer of tantalum is then masked. More particularly, photoresist is deposited over the backplate, and the photoresist is exposed. The tantalum layer is then etched. Because wet etch processes are not effective for etching tantalum, prior art processes must use a dry etch process. In one recent prior art process a reactive ion etch is used for etching the tantalum layer.

The use of two separate sputtering deposition steps is expensive and time consuming. Also, the use of two separate masking process steps is expensive and time consuming. These factors result in a low manufacturing yield and throughput. In addition, the steepness of the row electrodes and column electrodes of prior art processes results in manufacturing defects related to cracking of the overlying tantalum layer.

The dry etch process is complex. Also, the use of a dry etch process is expensive as it requires the use of expensive capital equipment (e.g. reactive ion etcher). Moreover, the dry etch process is corrosive to aluminum and can result in corrosion of the aluminum layer when pinholes are present in the tantalum layer. In addition, the dry etch process forms polymers within the tantalum layer. Thus, following the dry etch, a polymer strip process is required for removing the polymers. The polymer strip process is expensive. In addition, the corrosive dry etch process can result in pinholes in the glass backplate.

During subsequent conventional process steps, the column electrode is subjected to potential damage. More particularly damage often results from, ion bombardment, cavity etch, cone deposition, dielectric deposition,

masking and etching of the dielectric layer, deposition and etch of a molybdenum layer, deposition and etch of a chromium layer, polyimide deposition, etc. These process steps lead to shorts and opens that result in reduced yield and device failure.

Another problem that occurs in prior art devices is column to focus waffle shorts. These column to focus waffle shorts lead to reduced yield and device failure. In addition, the electrodes used in prior art column electrodes can react with the frit seal in the frit seal region, leading to shorts between column electrodes.

Thus, a need exists for an electrode structure and a method for forming an electrode structure that does not result in hillock formation. Still another need exists for an electrode structure and a method for forming an electrode structure that meets the above-listed needs but which does not produce undesired electrical shorts or opens in the cathode structure. Still another need exists for an electrode structure and a method for forming an electrode structure that meets the above-listed needs and that is inexpensive to manufacture and that does not result in reduced yield.

As yet another drawback, during fabrication of one embodiment of a multilayer electrode, a two step etch process is employed. In the first step, an oxidizing agent is used to oxidize the multilayer stack from which the multilayer electrode is to be formed. Next, an etchant is used which readily removes the oxidized material. The etchant is used to form the multilayer electrode from the multilayer stack of material. Unfortunately, when using

certain materials and under various circumstances, unwanted excess oxidation of the material comprising the multilayer stack can occur. This unwanted excess oxidation results in deleterious superfluous etching of the material in the multilayer stack. Hence, precise and controlled etching of the multilayer stack is compromised. Such compromising of the etching process can severely affect the formation of the electrode. In fact, "opens" or breaks in the multilayer electrode may result from unwanted excess oxidation and etching.

Thus, a need exists for a multilayer electrode and a method of forming such a multilayer electrode wherein the multilayer stack, from which the multilayer electrode is formed, is not subjected to unwanted excess oxidation during the electrode formation process. Still another need exists for a multilayer electrode and a method of forming such a multilayer electrode wherein the multilayer electrode does not suffer from excessive "opens" or breaks.

As still another drawback, during the formation of a multilayer electrode in a standard evacuated environment, it is possible to form intermetallic compounds. That is, the evacuated environment in which both layers of the multilayer stack is formed is conducive to the formation of intermetallic compounds. These intermetallic compounds are typically formed when atoms and molecules of the two separate metal layers diffuse together to form a new compound. Unfortunately, these intermetallic compounds have oxidation and etch rates which can vary greatly from that of the constituents which comprise the intermetallic compounds. As a

result, the formation of these intermetallic compounds can lead to variation and unpredictability in the subsequent oxidation and etching processes.

Thus, a need exists for a multilayer electrode and a method of forming such a multilayer electrode wherein the multilayer stack, from which the multilayer electrode is formed, does not suffer from significant formation of intermetallic compounds during the electrode formation process.

SUMMARY OF INVENTION

The present invention provides in one embodiment, an electrode structure and a method for forming an electrode structure that does not result in hillock formation. Also, the present invention provides an electrode structure and a method for forming an electrode structure that meets the above-listed need but which does not produce undesired electrical shorts or opens in the cathode structure. Also, the present invention provides an electrode structure and a method for forming an electrode structure that meets the above-listed needs and that is inexpensive and that increases yield and throughput.

In one embodiment of the present invention, an electrode structure for a flat panel display is shown that includes lower electrodes and upper electrodes. In the present embodiment, the lower electrodes are row electrodes and the upper electrodes are column electrodes. The lower electrodes and the upper electrodes are separated by a resistive layer and a dielectric layer. In one embodiment, both the upper electrodes and the lower electrodes are formed of a metal alloy. In one embodiment, the metal alloy is an aluminum alloy. Alternatively, a silver alloy is used.

A method for forming an electrode structure of a flat panel display is disclosed. First, a metal alloy layer is deposited over a backplate. A cladding layer is then deposited over the metal alloy layer. A wet etch step is then performed so as to form a layer of electrodes. By performing the deposition of the metal alloy layer and the cladding layer in the same sputtering tool sequentially, cost savings, increased yield and throughput result as compared to prior art processes that require two separate trips to a

sputtering tool. Moreover, because a single masking step and a single wet etch is required, significant cost savings, increased yield and throughput result as compared to prior art processes that require two separate masking steps and etch steps.

The present invention does not use a dry etch process. Thus, significant cost savings are realized because there is no need for complex and expensive capital equipment for performing the dry etch process. In addition, because the present invention does not use a dry etch process, there is no corrosion of an underlying aluminum layer and no damage (e.g. pinholes) to the glass backplate. Moreover, because the present invention does not use a dry etch process, there is no need to perform a polymer strip process. This results in further time and cost savings as compared to prior art processes and increased throughput and yield.

In one embodiment, a passivation layer is deposited over the upper electrode. In the present embodiment, the passivation layer is silicon nitride. The silicon nitride layer is then masked and etched. The resulting silicon nitride structure partially covers the upper electrodes. This protects the upper electrodes during subsequent process steps.

Gate metal is then deposited, masked and etched to form a gate structure. The passivation layer protects the upper electrodes during deposition, mask and etch steps. Conventional process steps are then used to complete the cathode structure. In one embodiment of the present conventional process steps are used to form emitters and to form a focusing structure. In the present embodiment, these process steps include ion

bombardment, cavity etch, cone deposition, dielectric deposition, masking and etching of the dielectric layer, deposition and etch of molybdenum layer, deposition and etch of chromium layer, polyimide deposition, etc. During these process steps, the upper electrodes are protected by the passivation layer. Thus, damage to upper electrodes is prevented. By preventing damage to upper electrodes, column shorts and opens are reduced. Also, because there is less exposed metal alloy, column to focus waffle shorts are decreased.

The use of either an aluminum alloy or the use of a silver alloy provides good conductivity. The resulting conductivity is sufficient for fabrication of large flat panel displays. In addition, the present invention prevents hillock formation as occurs in prior art processes that use aluminum. Thus, electrical shorts and opens are prevented as compared with prior art processes that use aluminum and good planarity of overlying layers is obtained. This results in increased yield as compared with prior art processes that use aluminum.

Thus, the present invention provides an electrode structure and a method for forming an electrode structure that does not result in hillock formation. Also, the present invention provides an electrode structure and a method for forming an electrode structure that meets the above-listed need but which does not produce undesired electrical shorts or opens in the cathode structure. Also, the present invention provides an electrode structure and a method for forming an electrode structure that meets the above-listed needs, that is inexpensive and that increases yield and throughput.

In still another embodiment the present invention provides a multilayer electrode and a method of forming such a multilayer electrode wherein the multilayer stack from which the multilayer electrode is formed is not subjected to unwanted excess oxidation during the electrode formation process. The present embodiment further provides a multilayer electrode and a method of forming such a multilayer electrode wherein the multilayer electrode does not suffer from excessive "opens" or breaks. Specifically, in such an embodiment, the multilayer electrode is formed by depositing a metal alloy layer. After the deposition of the metal alloy layer, the present embodiment deposits a protective layer over the metal alloy layer to form a multilayer stack. The present embodiment then subjects the multilayer stack to a cleansing process to remove contaminants. Subsequently, the present embodiment etches the multilayer stack to form the multilayer electrode for the flat panel display device.

In another embodiment, the present invention provides a multilayer electrode and a method of forming such a multilayer electrode wherein the multilayer stack, from which the multilayer electrode is formed, does not suffer from significant formation of intermetallic compounds during the electrode formation process. In such an embodiment, the present embodiment deposits a first metal alloy layer above a substrate. Next, the present embodiment forms a barrier layer above the first metal alloy layer. In this embodiment, the barrier layer is adapted to prevent the formation of an intermetallic compound within the first metal alloy layer. Next, the present embodiment deposits a second metal alloy layer above the barrier

layer. In so doing, the barrier layer also prevents the formation of the intermetallic compound within the second metal alloy layer.

These and other objects and advantages of the present invention will no doubt become obvious to those of ordinary skill in the art after having read the following detailed description of the preferred embodiments which are illustrated in the various drawing figures.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of this specification, illustrates embodiments of the invention and, together with the description, serve to explain the principles of the invention:

FIGURE 1 is a diagram showing a method for forming an electrode structure of a display device in accordance with one embodiment of the present invention.

FIGURE 2 is a side sectional view of a display device showing a backplate over which a metal alloy layer is deposited in accordance with one embodiment of the present invention.

FIGURE 3 is a side sectional view of a display device showing the deposition of a cladding layer in accordance with one embodiment of the present invention.

FIGURE 4A is a side sectional view of a display device showing an expanded view of the structure of Figure 3 after mask and etch steps have formed a lower electrode in accordance with one embodiment of the present claimed invention.

FIGURE 4B is a side sectional view of a display device showing an expanded view of the structure of Figure 3 after mask and etch steps have formed a lower electrode in accordance with one embodiment of the present claimed invention.

FIGURE 5A is a side sectional view of a display device showing the structure of Figure 4A after the deposition of a resistor layer in accordance with one embodiment of the present claimed invention.

FIGURE 5B is a side sectional view of a display device showing the structure of Figure 4B after the deposition of a resistor layer in accordance with one embodiment of the present claimed invention.

FIGURE 6A is a side sectional view of a display device showing the structure of Figure 5A after the deposition of a dielectric layer in accordance with one embodiment of the present claimed invention.

FIGURE 6B is a side sectional view of a display device showing the structure of Figure 5B after the deposition of a dielectric layer in accordance with one embodiment of the present claimed invention.

FIGURE 7A is a side sectional view of a display device showing the structure of Figure 6A after the deposition of a metal alloy layer in accordance with one embodiment of the present claimed invention.

FIGURE 7B is a side sectional view of a display device showing the structure of Figure 6B after the deposition of a metal alloy layer in accordance with one embodiment of the present claimed invention.

FIGURE 8A is a side sectional view of a display device showing the structure of Figure 7A after the deposition of a cladding layer in accordance with one embodiment of the present claimed invention.

FIGURE 8B is a side sectional view of a display device showing the structure of Figure 7B after the deposition of a cladding layer in accordance with one embodiment of the present claimed invention.

FIGURE 9A is a side sectional view of a display device showing the structure of Figure 8A after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 9B is a side sectional view of a display device showing the structure of Figure 8B after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 10A is a side sectional view of a display device showing the structure of Figure 9A after the deposition of a passivation layer in accordance with one embodiment of the present claimed invention.

FIGURE 10B is a side sectional view of a display device showing the structure of Figure 9B after the deposition of a passivation layer in accordance with one embodiment of the present claimed invention.

FIGURE 11A is a side sectional view of a display device showing the structure of Figure 10A after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 11B is a side sectional view of a display device showing the structure of Figure 10B after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 12A is a side sectional view of a display device showing the structure of Figure 11A after deposition of a gate metal layer in accordance with one embodiment of the present claimed invention.

FIGURE 12B is a side sectional view of a display device showing the structure of Figure 11B after deposition of a gate metal layer in accordance with one embodiment of the present claimed invention.

FIGURE 13A is a side sectional view of a display device showing the structure of Figure 12A after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 13B is a side sectional view of a display device showing the structure of Figure 12B after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 14A is a side sectional view of a display device showing the structure of Figure 13A after formation of emitters and focus structure in accordance with one embodiment of the present claimed invention.

FIGURE 14B is a side sectional view of a display device showing the structure of Figure 13B after formation of emitters and focus structure in accordance with one embodiment of the present claimed invention.

FIGURE 15 is a diagram showing a method for forming an electrode structure of a display device in accordance with one embodiment of the present invention.

FIGURE 16A is a side sectional view of a display device showing a backplate over which lower and upper electrodes are formed and having a resistor layer, a dielectric layer, and a gate structure in accordance with one embodiment of the present claimed invention.

FIGURE 16B is a side sectional view of a display device showing a backplate over which lower and upper electrodes are formed and having a resistor layer, a dielectric layer, and a gate structure in accordance with one embodiment of the present claimed invention.

FIGURE 16C is a side sectional view of a display device showing the structure of Figure 9A after deposition, mask and etch have formed a passivation layer in accordance with one embodiment of the present claimed invention.

FIGURE 16D is a side sectional view of a display device showing the structure of Figure 9B after deposition, mask and etch have formed a passivation layer in accordance with one embodiment of the present claimed invention.

FIGURE 16E is a side sectional view of a display device showing the structure of Figure 16C after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 16F is a side sectional view of a display device showing the structure of Figure 16D after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 16G is a side sectional view of a display device showing the structure of Figure 16E after evaporation of a chromium layer and deposition of cone material, deposition of a layer of dielectric material, and mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 16H is a side sectional view of a display device showing the structure of Figure 16F after evaporation of a chromium layer and deposition of cone material, deposition of a layer of dielectric material, and mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 16I is a side sectional view of a display device showing a completed cathode structure in accordance with one embodiment of the present claimed invention.

FIGURE 16J is a side sectional view of a display device showing a completed cathode structure in accordance with one embodiment of the present claimed invention.

FIGURE 17 is a diagram showing a method for forming an electrode structure of a display device in accordance with one embodiment of the present invention.

FIGURE 18A is a side sectional view of a display device showing a backplate over which lower and upper electrodes are formed and having a resistor layer, a dielectric layer, and a gate layer in accordance with one embodiment of the present claimed invention.

FIGURE 18B is a side sectional view of a display device showing a backplate over which lower and upper electrodes are formed and having a resistor layer, a dielectric layer, and a gate layer in accordance with one embodiment of the present claimed invention.

FIGURE 18C is a side sectional view of a display device showing the structure of Figure 18A after mask and etch steps have formed a gate structure in accordance with one embodiment of the present claimed invention.

FIGURE 18D is a side sectional view of a display device showing the structure of Figure 18B after mask and etch steps have formed a gate structure in accordance with one embodiment of the present claimed invention.

FIGURE 18E is a side sectional view of a display device showing the structure of Figure 18C after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 18F is a side sectional view of a display device showing the structure of Figure 18D after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 18G is a side sectional view of a display device showing the structure of Figure 18E after the deposition of a passivation layer and after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 18H is a side sectional view of a display device showing the structure of Figure 18F after the deposition of a passivation layer and after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 18I is a side sectional view of a display device showing the structure of Figure 18G after evaporation of a chromium layer and deposition of cone material, deposition of a layer of dielectric material, and mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 18J is a side sectional view of a display device showing the structure of Figure 18H after evaporation of a chromium layer and deposition of cone material, deposition of a layer of dielectric material, and

mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 18K is a side sectional view of a display device showing the structure of Figure 18I after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 18L is a side sectional view of a display device showing the structure of Figure 18J after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 18M is a side sectional view of a display device showing a completed cathode structure in accordance with one embodiment of the present claimed invention.

FIGURE 18N is a side sectional view of a display device showing a completed cathode structure in accordance with one embodiment of the present claimed invention.

FIGURE 19 is a diagram showing a method for forming an electrode structure of a display device in accordance with one embodiment of the present invention.

FIGURE 20A is a side sectional view of a display device showing a backplate over which lower and upper electrodes are formed and having a resistor layer, a dielectric layer, a tantalum layer, and a gate layer in accordance with one embodiment of the present claimed invention.

FIGURE 20B is a side sectional view of a display device showing a backplate over which lower and upper electrodes are formed and having a resistor layer, a dielectric layer, a tantalum layer and a gate layer in accordance with one embodiment of the present claimed invention.

FIGURE 20C is a side sectional view of a display device showing the structure of Figure 20A after mask and etch steps have formed a tantalum structure and a gate structure in accordance with one embodiment of the present claimed invention.

FIGURE 20D is a side sectional view of a display device showing the structure of Figure 20B after mask and etch steps have formed a tantalum structure and a gate structure in accordance with one embodiment of the present claimed invention.

FIGURE 20E is a side sectional view of a display device showing the structure of Figure 20C after the deposition of a passivation layer and after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 20F is a side sectional view of a display device showing the structure of Figure 20D after the deposition of a passivation layer and after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 20G is a side sectional view of a display device showing the structure of Figure 20E after evaporation of a chromium layer and deposition of cone material, deposition of a layer of dielectric material, and mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 20H is a side sectional view of a display device showing the structure of Figure 20F after evaporation of a chromium layer and deposition of cone material, deposition of a layer of dielectric material, and mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 20I is a side sectional view of a display device showing the structure of Figure 20G after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 20J is a side sectional view of a display device showing the structure of Figure 20H after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 20K is a side sectional view of a display device showing a completed cathode structure in accordance with one embodiment of the present claimed invention.

FIGURE 20L is a side sectional view of a display device showing a completed cathode structure in accordance with one embodiment of the present claimed invention.

FIGURE 21 is a diagram showing a method for forming an electrode structure of a display device in accordance with one embodiment of the present invention.

FIGURE 22A is a side sectional view of a display device showing a backplate over which lower and upper electrodes are formed and having a resistor layer, a dielectric layer, and a gate layer in accordance with one embodiment of the present claimed invention.

FIGURE 22B is a side sectional view of a display device showing a backplate over which lower and upper electrodes are formed and having a resistor layer, a dielectric layer, and a gate layer in accordance with one embodiment of the present claimed invention.

FIGURE 22C is a side sectional view of a display device showing the structure of Figure 22A after the deposition of a passivation layer and after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 22D is a side sectional view of a display device showing the structure of Figure 22B after the deposition of a passivation layer and after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 22E is a side sectional view of a display device showing the structure of Figure 22C after the deposition, mask and etch of a dielectric layer in accordance with one embodiment of the present claimed invention.

FIGURE 22F is a side sectional view of a display device showing the structure of Figure 22D after the deposition, mask and etch of a dielectric layer in accordance with one embodiment of the present claimed invention.

FIGURE 22G is a side sectional view of a display device showing the structure of Figure 22E after an etch step has been performed so as to form a cavity in accordance with one embodiment of the present claimed invention.

FIGURE 22H is a side sectional view of a display device showing the structure of Figure 22F after an etch step has been performed so as to form a cavity in accordance with one embodiment of the present claimed invention.

FIGURE 22I is a side sectional view of a display device showing the structure of Figure 22G after evaporation of a chromium layer and deposition of cone material, deposition of a layer of dielectric material, and mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 22J is a side sectional view of a display device showing the structure of Figure 22H after evaporation of a chromium layer and deposition of cone material, deposition of a layer of dielectric material, and

mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 22K is a side sectional view of a display device showing the structure of Figure 22I after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 22L is a side sectional view of a display device showing the structure of Figure 22J after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 22M is a side sectional view of a display device showing a completed cathode structure in accordance with one embodiment of the present claimed invention.

FIGURE 22N is a side sectional view of a display device showing a completed cathode structure in accordance with one embodiment of the present claimed invention.

FIGURE 23 is a diagram showing a method for forming an electrode structure of a display device in accordance with one embodiment of the present invention.

FIGURE 24A is a side sectional view of a display device showing a backplate over which lower and upper electrodes are formed and having a resistor layer, a dielectric layer, and a gate structure in accordance with one embodiment of the present claimed invention.

FIGURE 24B is a side sectional view of a display device showing a backplate over which lower and upper electrodes are formed and having a resistor layer, a dielectric layer, and a gate structure in accordance with one embodiment of the present claimed invention.

FIGURE 24C is a side sectional view of a display device showing the structure of Figure 24A after deposition of a sputtered molybdenum layer, deposition of an evaporated molybdenum layer, and deposition of a sputtered molybdenum layer in accordance with one embodiment of the present claimed invention.

FIGURE 24D is a side sectional view of a display device showing the structure of Figure 24B after deposition of a sputtered molybdenum layer, deposition of an evaporated molybdenum layer, and deposition of a sputtered molybdenum layer in accordance with one embodiment of the present claimed invention.

FIGURE 24E is a side sectional view of a display device showing the structure of Figure 24C after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 24F is a side sectional view of a display device showing the structure of Figure 24D after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 24G is a side sectional view of a display device showing the structure of Figure 24E after deposition of a dielectric layer and a passivation layer in accordance with one embodiment of the present claimed invention.

FIGURE 24H is a side sectional view of a display device showing the structure of Figure 24F after deposition of a dielectric layer and a passivation layer in accordance with one embodiment of the present claimed invention.

FIGURE 24I is a side sectional view of a display device showing the structure of Figure 24G after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 24J is a side sectional view of a display device showing the structure of Figure 24H after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 24K is a side sectional view of a display device showing the structure of Figure 24I after mask and etch steps have been performed and after focusing structures have been formed in accordance with one embodiment of the present claimed invention.

FIGURE 24L is a side sectional view of a display device showing the structure of Figure 24J after mask and etch steps have been performed and after focusing structures have been formed in accordance with one embodiment of the present claimed invention.

FIGURE 24M is a side sectional view of a display device showing the structure of Figure 24K after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 24N is a side sectional view of a display device showing the structure of Figure 24L after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 25 is a diagram showing a method for forming an electrode structure of a display device in accordance with one embodiment of the present invention.

FIGURE 26A is a side sectional view of a display device showing a backplate over which lower and upper electrodes are formed and having a resistor layer, a dielectric layer, a gate structure, a sputtered molybdenum layer, an evaporated molybdenum layer, and a sputtered molybdenum layer, after mask and etch steps and after the deposition of a dielectric layer in accordance with one embodiment of the present claimed invention.

FIGURE 26B is a side sectional view of a display device showing a backplate over which lower and upper electrodes are formed and having a resistor layer, a dielectric layer, a gate structure, a sputtered molybdenum layer, an evaporated molybdenum layer, and a sputtered molybdenum layer, after mask and etch steps and after the deposition of a dielectric layer in accordance with one embodiment of the present claimed invention.

FIGURE 26C is a side sectional view of a display device showing the structure of Figure 26A after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 26D is a side sectional view of a display device showing the structure of Figure 26B after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 26E is a side sectional view of a display device showing the structure of Figure 26C after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 26F is a side sectional view of a display device showing the structure of Figure 26D after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 26G is a side sectional view of a display device showing the structure of Figure 26E after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 26H is a side sectional view of a display device showing the structure of Figure 26F after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 26I is a side sectional view of a display device showing the structure of Figure 26G after mask and etch steps and formation of a

focusing structure in accordance with one embodiment of the present claimed invention.

FIGURE 26J is a side sectional view of a display device showing the structure of Figure 26H after mask and etch steps and formation of a focusing structure in accordance with one embodiment of the present claimed invention.

FIGURE 26K is a side sectional view of a display device showing the structure of Figure 26I after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 26L is a side sectional view of a display device showing the structure of Figure 26J after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 27 is a diagram showing a method for forming an electrode structure of a display device in accordance with one embodiment of the present invention.

FIGURE 28A is a side sectional view of a display device showing a backplate over which lower and upper electrodes are formed and having a resistor layer, a dielectric layer, a gate structure, an evaporated chromium layer, an evaporated molybdenum layer, and a dielectric layer in accordance with one embodiment of the present claimed invention.

FIGURE 28B is a side sectional view of a display device showing a backplate over which lower and upper electrodes are formed and having a resistor layer, a dielectric layer, a gate structure, an evaporated chromium layer, an evaporated molybdenum layer, and a dielectric layer in accordance with one embodiment of the present claimed invention.

FIGURE 28C is a side sectional view of a display device showing the structure of Figure 28A after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 28D is a side sectional view of a display device showing the structure of Figure 28B after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 28E is a side sectional view of a display device showing the structure of Figure 28C after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 28F is a side sectional view of a display device showing the structure of Figure 28D after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 28G is a side sectional view of a display device showing the structure of Figure 28E after focusing structures have been formed in accordance with one embodiment of the present claimed invention.

FIGURE 28H is a side sectional view of a display device showing the structure of Figure 28F focusing structures have been formed in accordance with one embodiment of the present claimed invention.

FIGURE 28I is a side sectional view of a display device showing the structure of Figure 28G after an etch step has been performed in accordance with one embodiment of the present claimed invention.

FIGURE 28J is a side sectional view of a display device showing the structure of Figure 28H after an etch step has been performed in accordance with one embodiment of the present claimed invention.

FIGURE 28K is a side sectional view of a display device showing the structure of Figure 28I after an etch step has been performed in accordance with one embodiment of the present claimed invention.

FIGURE 28L is a side sectional view of a display device showing the structure of Figure 26J after an etch step has been performed in accordance with one embodiment of the present claimed invention.

FIGURE 29A is a side sectional view illustrating the deposition of a metal alloy layer during the formation of a multilayer electrode in accordance with one embodiment of the present claimed invention.

FIGURE 29B is a side sectional view of the structure of FIGURE 29A after the deposition of a protective layer thereon in accordance with one embodiment of the present claimed invention.

FIGURE 29C is a side sectional view of the structure of FIGURE 29B prior to having contaminants removed therefrom in accordance with one embodiment of the present claimed invention.

FIGURE 29D is a side sectional view of the structure of FIGURE 29C subsequent to subjecting the structure of FIGURE 29C to a cleansing process in accordance with one embodiment of the present claimed invention.

FIGURE 29E is a side sectional view of the structure of FIGURE 29D having a layer of photoresist disposed thereon in accordance with one embodiment of the present claimed invention.

FIGURE 29F is a side sectional view of the structure of FIGURE 29E having a patterned layer of photoresist disposed thereon in accordance with one embodiment of the present claimed invention.

FIGURE 29G is a side sectional view of the structure of FIGURE 29F subsequent to subjecting the structure of FIGURE 29F to an etching step in accordance with one embodiment of the present claimed invention.

FIGURE 29H is a side sectional view of a multilayer electrode in accordance with one embodiment of the present claimed invention.

FIGURE 30 is a flow chart of steps associated with the formation of a multilayer electrode in accordance with one embodiment of the present claimed invention.

FIGURE 31A is a side sectional view illustrating the deposition of a first metal alloy layer during the formation of a multilayer electrode in accordance with one embodiment of the present claimed invention.

FIGURE 31B is a side sectional view of the structure of FIGURE 31A after the formation of a barrier layer thereon in accordance with one embodiment of the present claimed invention.

FIGURE 31C is a side sectional view of the structure of FIGURE 31B after the deposition of a second metal alloy layer thereon in accordance with one embodiment of the present claimed invention.

FIGURE 31D is a side sectional view of the structure of FIGURE 31C prior to having contaminants removed therefrom in accordance with one embodiment of the present claimed invention.

FIGURE 31E is a side sectional view of the structure of FIGURE 31D subsequent to subjecting the structure of FIGURE 31D to a cleansing process in accordance with one embodiment of the present claimed invention.

FIGURE 31F is a side sectional view of the structure of FIGURE 31E having a layer of photoresist disposed thereon in accordance with one embodiment of the present claimed invention.

FIGURE 31G is a side sectional view of the structure of FIGURE 31F having a patterned layer of photoresist disposed thereon in accordance with one embodiment of the present claimed invention.

FIGURE 31H is a side sectional view of the structure of FIGURE 31G subsequent to subjecting the structure of FIGURE 31G to an etching step in accordance with one embodiment of the present claimed invention.

FIGURE 31I is a side sectional view of a multilayer electrode in accordance with one embodiment of the present claimed invention.

FIGURE 32 is a flow chart of steps associated with the formation of a multilayer electrode with reduced intermetallic compound formation in accordance with one embodiment of the present claimed invention.

The drawings referred to in this description should be understood as not being drawn to scale except if specifically noted.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to the preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the preferred embodiments, it will be understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be obvious to one of ordinary skill in the art that the present invention may be practiced without these specific details. In other instances, well known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the present invention.

With reference now to Figure 1, a method for forming an electrode structure for a display device is shown. As shown by step 101, a metal alloy layer is deposited. Figure 2 shows a metal alloy layer 2 deposited over glass plate 1.

In one embodiment, metal alloy layer 2 is an aluminum alloy. In one embodiment, metal alloy layer 2 has a thickness of 500-5000 Angstroms. In one specific embodiment, an aluminum alloy is used that includes aluminum (Al) and Neodymium (Nd). In the present embodiment, the aluminum alloy has an concentration of from .5 to 6 atomic percent Nd. In

another embodiment, an aluminum alloy is used that has a concentration of from .5 to 6 atomic percent Nd and from 0 to 5 atomic percent titanium (Ti).

Continuing with Figures 1-2, in an alternate embodiment, metal alloy layer 2 is a silver alloy. In one embodiment a silver alloy is used that includes silver (Ag) and .5 to 2 atomic percent palladium (Pd) and .5 to 2 atomic percent copper (Cu). In yet another embodiment, a silver alloy is used that includes .5 percent to 2 atomic percent palladium and 0.0 to 2.0 atomic percent titanium.

When a silver alloy is used, an adhesion layer can be used to promote adhesion to the glass plate. In one embodiment, a molybdenum adhesion layer is used that has a thickness of approximately 500-1000 angstroms.

Referring to Figure 1, as shown by step 102, a cladding layer is then deposited. Figure 3 shows the structure of Figure 2 after cladding layer 3 has been deposited. It can be seen that cladding layer 3 directly overlies metal alloy layer 2.

In one embodiment, cladding layer 3 of Figure 3 is a molybdenum (Mo) tungsten (W) alloy. In the present embodiment, cladding layer 3 has a thickness of approximately 500-4000 angstroms. The use of cladding layer 3 produces a contact pad that is reliable and that maintains good electrical contact. In addition, the use of cladding layer 3 further reduces hillock formation. In the present embodiment, the molybdenum alloy has a concentration of from 5-30 atomic percent tungsten.

Though the present invention includes the deposition of cladding layer 3, the present invention is well adapted for use without cladding layer 3. That is, the use of aluminum alloy or silver alloy provides sufficient reduction in hillock formation and results in good conductivity as compared with prior art processes.

In one embodiment, a diffusion barrier layer is used. The diffusion barrier layer can be formed of is titanium, titanium nitride or titanium tungsten that is deposited directly over the silver alloy. In one embodiment, a diffusion barrier layer is used that has a thickness of approximately 500-2000 Angstroms. The use of a diffusion barrier layer is particularly useful in an embodiment that does not include a cladding layer.

In one embodiment, the deposition of metal alloy layer 2 and cladding layer 3 is conducted using a single sputtering tool. That is, in the present invention, a sputtering process is used whereby metal alloy layer 2 and cladding layer 3 are sequentially deposited in a single sputtering tool. More particularly, in one embodiment, glass plate 1 is placed into a sputtering tool that includes a sputtering chamber that first deposits metal alloy layer 2 and then deposits cladding layer 3. The glass plate is then removed from the sputtering chamber. This provides significant cost savings over prior art methods that require two separate sputtering process steps and results in increased throughput and yield.

The use of either an aluminum alloy or the use of a silver alloy in conjunction with a cladding layer provides good conductivity. The resulting

conductivity is sufficient for fabrication of large flat panel displays. In addition, the present invention prevents hillock formation as occurs in prior art processes that use aluminum. Thus, shorts are prevented as compared with prior art processes that use aluminum and planarity of overlying layers is obtained. This results in increased yield as compared with prior art processes that use aluminum.

Referring back to Figure 1, mask and etch steps are performed as shown by step 103. More particularly, in the present embodiment, photoresist is deposited over the backplate and is patterned. The backplate is then etched using a wet etch process to form the desired row electrodes. Figures 4A-4B show the structure of Figure 3 after mask and etch steps have formed exemplary lower electrode 4.

The present invention requires a single patterning step and a single etch step in order to form row electrodes. Thus, the present invention does not require two separate patterning steps as are required in prior art processes. This results in significant cost savings as compared to prior art processes that require two separate patterning steps. In addition, because the present invention does not require two separate etch steps as are required in prior art processes that use a molybdenum cap, the present invention results in increased yield and throughput.

The present invention does not use a dry etch process for forming row electrodes. Thus, significant cost savings are realized because there is no need for complex and expensive capital equipment for performing the dry etch process. In addition, because the present invention does not use a dry

etch process, there is no corrosion of an underlying aluminum layer and no damage (e.g. pinholes) to the glass backplate. Moreover, because the present invention does not use a dry etch process, there is no need to perform a polymer strip process. This results in further increases in throughput and yield as compared to prior art processes.

In one embodiment, the etching process forms angled edges. In the present embodiment, an etchant is used that includes nitric acid, phosphoric acid, ascetic acid and water. The use of this etchant performs a controlled lifting of the photoresist and results in angled edges on the sides of the lower electrode 4. The use of angled edges results in good conformity of overlying layers and reduces cracking in overlying layers.

Referring back to Figure 1, a resistor layer is deposited as shown by step 104. In the embodiment shown in Figures 5A-5B, resistor layer 5 is shown to overlie lower electrode 4. In one embodiment, resistor layer 5 has a thickness of approximately 2000-4000 angstroms. In the present embodiment, resistor layer 5 is silicon carbide (SiC)that is either deposited using a sputtering process or a chemical vapor deposition process to a thickness of 2000-4000 angstroms.

A layer of dielectric is then deposited as shown by step 105 of Figure 1. In one embodiment silicon dioxide (SiO2) is used as a dielectric. In the present embodiment, a plasma enhanced chemical vapor deposition process is used to deposit the silicon dioxide layer. Referring now to Figures 6A-6B, the embodiment of Figures 5A-5B is shown after the deposit of dielectric layer 6.

A metal alloy layer is then deposited as shown by step 106 of Figure 1. In the present embodiment, the metal alloy layer has a thickness of approximately 500-5000 Angstroms. Figures 7A-7B show metal alloy layer 11 deposited over dielectric layer 6. In one embodiment, metal alloy layer 11 is an aluminum alloy. More particularly, in one specific embodiment, an aluminum alloy is used that includes aluminum and from .5 to 6 atomic percent neodymium and from 0 to 5 atomic percent titanium.

Alternatively, metal alloy layer 11 is a silver alloy. In one embodiment, metal alloy layer 11 includes silver and .5 to 2 atomic percent palladium and .5 to 2 atomic percent copper. In yet another embodiment, a silver alloy is used that includes .5 percent to 2 atomic percent palladium Pd and 0.0 to 2.0 atomic percent titanium.

When a silver alloy is used an adhesion layer can be used to promote adhesion to the gate structure. In one embodiment, a molybdenum adhesion layer is used that has a thickness of approximately 500-1000 angstroms is used.

Referring to Figure 1, as shown by step 107, a cladding layer is then deposited. Figure 8A-8B shows the structure of Figures 7A-7B after cladding layer 12 has been deposited. It can be seen that cladding layer 12 directly overlies metal alloy layer 11.

In one embodiment, cladding layer 12 of Figure 3 is a molybdenum tungsten alloy. In the present embodiment, cladding layer 12 has a

thickness of approximately 500 -4000 angstroms. The use of cladding layer 12 produces a contact pad that is reliable and that maintains good electrical contact. In addition, the use of cladding layer 12 further reduces hillock formation.

Though the present invention includes the deposition of cladding layer 12, the present invention is well adapted for use without cladding layer 12. That is, the use of aluminum alloy or silver alloy provides sufficient reduction in hillock formation and results in good conductivity as compared with prior art processes. In an embodiment that does not include cladding layer 12 but which uses a silver alloy, a diffusion barrier layer can be used. In one embodiment, the diffusion barrier layer is titanium or titanium nitride or titanium tungsten that is deposited over the silver alloy and that has a thickness of approximately 500-2000 Angstroms.

In one embodiment, the deposition of metal alloy layer 11 and cladding layer 12 is conducted using a single sputtering tool. This provides significant cost savings over prior art methods that require two separate sputtering process steps and results in increased throughput and yield.

Referring to step 108 of Figure 1, mask and etch steps are performed for forming upper electrodes. In the present invention, a wet etch process is used. Figure 9A-9B show the structure of Figures 8A-8B after mask and etch steps have formed exemplary upper electrode 14. In one embodiment, an etchant is used that includes nitric acid, phosphoric acid, ascetic acid and water for forming angled edges on the sides of upper electrode 14. The

use of an angled edges results in good conformity of overlying layers and reduces cracking in overlying layers.

The use of either an aluminum alloy or the use of a silver alloy in conjunction with a cladding layer provides good conductivity. The resulting conductivity is sufficient for fabrication of large flat panel displays. In addition, the present invention prevents hillock formation as occurs in prior art processes that use aluminum. Thus, shorts are prevented as compared with prior art processes that use aluminum and planarity of overlying layers is obtained. This results in increased yield as compared with prior art processes that use aluminum. Moreover, the present invention requires a single patterning step and a single etch step in order to form upper electrode 14. Thus, the present invention does not require two separate patterning steps and two separate etch steps as are required in prior art processes. This results in significant cost savings and increased yield and throughput. Also, the present invention does not use a dry etch process. This results in cost savings and increases in yield and throughput.

Referring now to step 109 of Figure 1, a passivation layer is deposited. In one embodiment, the passivation layer is silicon nitride deposited using a plasma enhanced chemical vapor deposition process. Referring now to Figure 10A-10B, the structure of Figure 9A-9B is shown after passivation layer 15 is deposited.

Referring now to step 110 of Figure 1, mask and etch steps are performed. Figures 11A-11B show the structure of Figures 10A-10B after

mask and etch steps have formed openings 16-18. It can be seen that passivation layer 15 extends over upper electrode 14 except at openings 17-18.

Gate metal is then deposited as shown by step 111 of Figure 1. In one embodiment, chromium is used as a gate metal. Figures 12A-12B show the structure of Figure 11A-11B after gate metal layer 20 has been deposited. In an alternate embodiment, gate metal layer 20 is formed by first depositing a tantalum layer and then depositing a chromium layer over the tantalum layer. Passivation layer 15 protects upper electrode 14 during the deposition of gate metal layer 20.

Referring now to step 112 of Figure 1, mask and etch steps are performed to form a gate structure. Figure 13A-13B show the structure of Figures 11A-11B after mask and etch steps have formed gate structure 21. In the present embodiment, column contact pad 22 allows for contact with upper electrode 14. Passivation layer 15 protects upper electrode 14 during mask and etch steps for forming gate metal structure 21.

Conventional process steps are then used to complete the cathode structure as shown by step 113 of Figure 1. Figure 14A-14B show a completed cathode structure according to one embodiment of the present invention. In one embodiment of the present conventional process steps are used to form cavity 221 and to form exemplary emitter 26 within cavity 221. Mask and etch steps are used to extend opening 16 of Figure 11B so as to expose row contact pad 23. Conventional process steps are also used to form focusing structure 24 and focus waffle metal 27. In one embodiment, focus

waffle metal 27 is aluminum. In the present invention, these process steps include ion bombardment, cavity etch, cone deposition, dielectric deposition, masking and etching of the dielectric layer, polyimide deposition, etc.

During the process steps for completion of the cathode, upper electrode 14 is protected by passivation layer 15. This prevents damage to upper electrode 14 as typically occurs in prior art processes. By preventing damage to upper electrode 14, upper electrode shorts and opens are prevented. In addition, because upper electrode 14 is protected, column shorts in the frit seal region are eliminated. Also, because there is less exposed metal as compared with prior art processes, column to focus waffle shorts are decreased.

With reference now to Figures 15a-f, a second embodiment of a method for forming an electrode structure for a display device is shown. As shown by step 101 a metal alloy layer is deposited. As shown by step 102, a cladding layer is then deposited. Mask and etch steps are performed as shown by step 103 to form lower electrodes. A resistor layer is deposited as shown by step 104. A layer of dielectric is then deposited as shown by step 105. A metal alloy layer is then deposited as shown by step 106. As shown by step 107, a cladding layer is then deposited. Referring to step 108, mask and etch steps are performed for forming upper electrodes. In one embodiment, steps 101-108 are identical to steps 101-108 of Figure 1, producing the structure shown in Figures 9A-9B.

Referring now to step 111 of Figure 15, a gate metal layer is deposited. The gate metal layer is then masked and etched as shown by step 112. Referring now to Figure 16a-b, the structure of Figures 9a-9b is shown after steps 111-112 have been performed so as to form gate structure 1601. In one embodiment, gate structure 1601 is chromium. Alternatively, gate structure 1601 is a layer of chromium deposited over a layer of tantalum.

Continuing with Figure 15, as shown by steps 109-110, a passivation layer is deposited, masked and etched. Figure 16c-16d show the structure of Figure 16a-16b after steps 109-110 have formed passivation layer 1602. In one embodiment, passivation layer 1602 is silicon nitride deposited using a plasma enhanced chemical vapor deposition process. Openings 1620-1621 extend through passivation layer 1602. It can be seen that passivation layer 1602 extends over gate structure 1601 except at openings 1620-1621.

The cathode structure is then completed as shown by step 113 of Figure 15. Figures 16E-16J illustrate an exemplary method for completing the cathode structure in accordance with one embodiment of the present invention. First an etch step is performed. Figures 16E-16F show the structure of Figures 16C-16D after the etch step has formed cavity 25. A layer of chromium is evaporated over the structure, followed by the deposition of cone material and the deposition of a dielectric layer. In one embodiment, the layer of chromium is thin, having a thickness of approximately 500 Angstroms. The resulting structure is then patterned and etched so as to produce the structure shown in Figures 16G-16H. The structure of Figures 16G-16H shows dielectric material 1654, cone 26, cone material 1653 and chromium 1640. In one embodiment, cone material 1653

is evaporated molybdenum. However, the present invention is well adapted for use of other materials for forming cone 26. Mask and etch steps form opening 1656 that exposes portions of lower electrode 4 so as to form lower contact pad 23. Dielectric removal steps and a halo etch are then performed, followed by formation of polyimide structures and focus waffle metal. Figures 16I-16J show a completed cathode structure that includes polyimide structures 24, focus waffle metal 27 and upper contact pad 22.

During the process steps for completion of the cathode, upper electrode 14 is protected by gate metal structure 1601 and by passivation layer 15. This prevents damage to upper electrode 14 as typically occurs in prior art processes. By preventing damage to upper electrode 14, upper electrode shorts and opens are prevented. In addition, because upper electrode 14 is protected, column shorts in the frit seal region are eliminated. Also, because there is less exposed metal as compared with prior art processes, column to focus waffle shorts are decreased.

With reference now to Figure 17, yet another method for forming an electrode structure for a display device is shown. As shown by step 201, lower electrodes are formed over a substrate. A resistor layer and a dielectric layer are then deposited over the lower electrodes as shown by steps 202-203. In one embodiment, steps 201-203 are identical to steps 101-105 of Figure 1.

Continuing with Figure 17, gate metal is deposited as is shown by step 204. In one embodiment, chromium is used as a gate metal.

Referring still to Figure 17, upper electrodes are formed as shown by step 205. In the one embodiment, upper electrodes are formed in the same manner as shown in steps 106-108 of Figures 1 and 15. In the present embodiment, upper electrodes are formed by depositing a metal alloy layer that is an aluminum alloy and masking and etching the metal alloy layer. In one specific embodiment, a metal alloy layer is used that a thickness of 500-5000 Angstroms and that includes aluminum (Al) and Neodymium (Nd) with a concentration of from .5 to 6 atomic percent Nd. In another embodiment, an aluminum alloy is used that has a concentration of from .5 to 6 atomic percent Nd and from 0 to 5 atomic percent titanium (Ti).

Figures 18A-18B show substrate 1 after steps 201-205 have been performed, forming lower electrodes 4 over substrate 1, resistor layer 5, dielectric layer 6, gate metal layer 1801 and upper electrodes 1810.

Referring back to Figure 17, as shown by step 206, mask and etch steps are then performed so as to selectively etch gate metal layer 1801 of Figure 18A-18B. More particularly, in the present embodiment, photoresist is deposited over the backplate and is patterned. The backplate is then etched using a wet etch process. Figures 18C-18D show the structure of Figures 18A-18B after mask and etch steps have formed gate metal structure 1811.

Referring now to step 207 of Figure 17, a passivation layer is deposited. In one embodiment, the passivation layer is silicon nitride deposited using a plasma enhanced chemical vapor deposition process.

Referring now to step 208 of Figure 17, mask and etch steps are performed. Referring now to Figure 18E-18F, the structure of Figure 18C-18D is shown after a passivation layer is deposited, masked and etched to form openings 1820 and 1821 that extend through passivation layer 1830. In one embodiment of the present invention, cavity 1825 is also formed using a HALO etch. It can be seen that passivation layer 1830 extends over upper electrode 1810 except at opening 1820.

The cathode structure is then completed as shown by step 209 of Figure 17. Figures 18G-18N illustrate an exemplary method for completing the cathode in accordance with one embodiment of the present invention. Mask and etch steps are performed to form a cavity, shown in Figure 18G as cavity 1825. A layer of chromium is evaporated over the structure, followed by the deposition of cone material and the deposition of a dielectric layer. The resulting structure is then patterned and etched so as to produce the structure shown in Figures 18I-18J. More particularly, cone 1826 and structures 1891 and 1892 are formed. Structures 1891 and 1892 include cone material 1853, chromium material 1840 and dielectric material 1854. Mask and etch steps then form openings that expose portions of lower electrode 4 so as to form lower contact pad 1856 as shown in Figures 18K-18L. Dielectric removal steps and a halo etch are then performed, followed by formation of polyimide structures and focus waffle metal. Figures 18M-18N show a completed cathode structure that includes upper contact pad 1857, focusing structures 1824 and focus waffle metal 1827. In an alternate embodiment of the present invention (not shown) mask and etch steps do not form structure 1892. That is, only structure 1891 is formed.

During the process steps for completion of the cathode, upper electrode 1810 is protected by passivation layer 1830. This prevents damage to upper electrode 1810 as typically occurs in prior art processes. By preventing damage to upper electrode 1810, upper electrode shorts and opens are prevented. In addition, because upper electrode 1810 is protected, column shorts in the frit seal region are eliminated. Also, because there is less exposed metal as compared with prior art processes, column to focus waffle shorts are decreased.

With reference now to Figure 19, yet another method for forming an electrode structure for a display device is shown. As shown by step 201 lower electrodes are formed over a substrate. A resistor layer and a dielectric layer are then deposited over the lower electrodes as shown by steps 202-203.

Continuing with Figure 19, gate metal is deposited as is shown by step 204. In one embodiment, chromium is used as a gate metal.

Referring still to Figure 19, a tantalum layer is deposited as shown by step 250. Upper electrodes are then formed as shown by step 205. In the present embodiment, upper electrodes are formed using an aluminum alloy. In one embodiment, the metal alloy has a thickness of 500-5000 Angstroms. In one specific embodiment, an aluminum alloy is used that includes aluminum (Al) and Neodymium (Nd). In the present embodiment, the aluminum alloy has an concentration of from .5 to 6 atomic percent Nd. In another embodiment, an aluminum alloy is used

that has a concentration of from .5 to 6 atomic percent Nd and from 0 to 5 atomic percent titanium (Ti).

Figures 18a-18b show substrate 1 after steps 201-205 and 250 have been performed, forming a gate metal layer 1801, a tantalum layer 1802, and upper electrodes 1810. In one embodiment, lower electrode 4 is a row electrode and upper electrode 1810 is a column electrode. However, alternatively, the present invention is well adapted to use of lower electrode 4 as a column electrode and upper electrode 1810 as a row electrode.

Referring back to Figure 19, as shown by step 252, mask and etch steps are then performed so as to selectively etch tantalum layer 1802 and gate metal layer 1801 of Figure 20A-20B. More particularly, in the present embodiment, photoresist is deposited over the backplate and is patterned. The backplate is then etched using a wet etch process. Figures 20C-20D show the structure of Figures 20A-20B after mask and etch steps have formed gate metal structure 1811 and tantalum structure 1812.

Referring now to step 207 of Figure 19, a passivation layer is deposited. In one embodiment, the passivation layer is silicon nitride deposited using a plasma enhanced chemical vapor deposition process.

Referring now to step 208 of Figure 19, mask and etch steps are performed. Referring now to Figure 20E-20F, the structure of Figure 20C-20D is shown after a passivation layer is deposited, masked and etched to formed opening 1820 that extends through passivation layer 1830 and tantalum structure 1812. In one embodiment of the present invention, a

halo etch is also performed, forming cavity 1825. It can be seen that passivation layer 1830 extends over upper electrode 1810 except at opening 1820. Passivation layer 1830 protects upper electrode 1810 during subsequent process steps.

The cathode structure is then completed as shown by step 209 of Figure 19. Figures 20G-20L illustrate an exemplary method for completing the cathode structure in accordance with one embodiment of the present invention. A layer of chromium is evaporated over the structure, followed by the deposition of cone material and the deposition of a dielectric layer. The resulting structure is then patterned and etched so as to produce the structure shown in Figures 20G-20H. The structure of Figures 20G-20H includes dielectric material 1854, cone 1826, cone material 1853 and chromium segment 1840. In one embodiment, cone material 1853 is evaporated molybdenum. However, the present invention is well adapted for use of other materials for forming cone 1826. Mask and etch steps then form openings 1856-1857 that expose portions of lower electrode 4 and upper electrode 1810 so as to form lower contact pad 1823 and upper contact pad 1822 as shown in Figures 20I-20J. Dielectric removal steps and a halo etch are then performed, followed by formation of polyimide structures and focus waffle metal. Figures 20K-20L show a completed cathode structure that includes polyimide structures 1824 and focus waffle metal 1827.

During the process steps for completion of the cathode, upper electrode 1810 is protected by passivation layer 1830. This prevents damage to upper electrode 1810 as typically occurs in prior art processes. By preventing damage to upper electrode 1810, upper electrode shorts and

opens are prevented. In addition, because upper electrode 1810 is protected, column shorts in the frit seal region are eliminated. Also, because there is less exposed metal as compared with prior art processes, column to focus waffle shorts are decreased.

With reference now to Figure 21, yet another method for forming an electrode structure for a display device is shown. As shown by steps 201, lower electrodes are formed over a substrate. A resistor layer and a dielectric layer are then deposited over the lower electrodes as shown by steps 202-203.

Continuing with Figure 21, gate metal is deposited as is shown by step 204. In one embodiment, chromium is used as a gate metal. Upper electrodes are then formed as shown by step 205. In the present embodiment, upper electrodes are formed of an aluminum alloy. In one embodiment, steps 201-205 are identical to steps 201-205 of Figure 17.

Referring now to Figures 22A-22B, a substrate 1 is shown after steps 201-205 have formed a gate metal layer 1801 and upper electrodes 1810 that overlie dielectric layer 6, resistor layer 5 and lower electrode 4.

Referring now to step 207 of Figure 21, a passivation layer is deposited. In one embodiment, the passivation layer is silicon nitride deposited using a plasma enhanced chemical vapor deposition process. Alternatively, a tantalum layer can be used.

Referring back to Figure 21, as shown by step 260, mask and etch steps are then performed. In one embodiment, a two step etch process is used whereby the passivation layer is etched using a first etch step and the gate metal layer is etched in a second etch step. The first mask and etch step etches through the passivation layer and etches through the gate metal layer. Figures 22C-22D show the structure of Figures 22A-22B after mask and etch steps have formed gate metal structure 1811 and passivation layer 1830.

The cathode structure is then completed as shown by step 209 of Figure 21. Figures 22E-22N illustrate an exemplary method for completing the cathode in accordance with one embodiment of the present invention. A dielectric layer is deposited over the structure of Figures 22C-22D. The dielectric layer 2250 is then patterned and etched to form the structure shown in Figures 22E-22F. During the etch process, passivation layer 1830 acts as an etch stop. A cavity etch is then performed. Figures 22G-22H show the structure of Figures 22E-22F after the cavity etch has formed cavity 1825.

A layer of Molybdenum is then deposited, using a sputter deposition process. A layer of cone material is then deposited over the layer of Molybdenum. In one embodiment, a cone material that is evaporated molybdenum is used. However, the present invention is well adapted for use of other materials for forming a cone. A layer of dielectric is then deposited. The resulting structure is then patterned and etched so as to produce the structure shown in Figures 22I-22J. The structure of Figures 22I-22J includes Molybdenum structure 2252, cone 2226, cone material 2253

and dielectric layer 2254. Mask and etch steps then form openings 2256-2257 shown in Figures 22K-22L. Referring now to Figures 22M-22N, dielectric removal steps and a halo etch are then performed, producing contact pads 2222 and 2223, followed by formation of polyimide focusing structures 2224 and focus waffle metal 2227.

During the process steps for completion of the cathode, upper electrode 1810 is protected by passivation layer 1830. This prevents damage to upper electrode 1810 as typically occurs in prior art processes. By preventing damage to upper electrode 1810, upper electrode shorts and opens are prevented. In addition, because upper electrode 1810 is protected, column shorts in the frit seal region are eliminated. Also, because there is less exposed metal as compared with prior art processes, upper electrode to focus waffle shorts are decreased.

With reference now to Figures 23-24, yet another method for forming an electrode structure for a display device is shown. As shown by step 201 of Figure 23, lower electrodes are formed over a substrate. A resistor layer and a dielectric layer are then deposited over the lower electrodes as shown by steps 202-203. A gate metal layer is deposited as shown by step 204, followed by the formation of upper electrodes as shown by step 205. An etch step is then performed to form a gate structure as shown by step 206 followed by etch step 2301 to form a cavity.

In the present embodiment, upper electrodes are formed by the deposition and etch of a metal alloy layer. In one embodiment, the metal alloy is an aluminum alloy that has a thickness of 500-5000 Angstroms. In

one specific embodiment, an aluminum alloy is used that includes aluminum (Al) and Neodymium (Nd). In the present embodiment, the aluminum alloy has an concentration of from .5 to 6 atomic percent Nd. In another embodiment, an aluminum alloy is used that has a concentration of from .5 to 6 atomic percent Nd and from 0 to 5 atomic percent titanium (Ti).

Referring to Figure 24A-24B, a substrate 1 is shown after steps 201-206 have formed lower electrodes 4, resistor layer 5, dielectric layer 6, gate metal structure 1811 and upper electrodes 1810. Etch step 2301 forms cavity 2425.

Continuing with Figure 23, a layer of sputtered molybdenum is then deposited as shown by step 2302. A layer of evaporated molybdenum is then deposited as shown by step 2303, followed by the deposition of a layer of sputtered molybdenum as shown by step 2304. Referring now to Figure 24C-24D, the structure of Figures 24A-24B is shown after steps 2302-2304 form sputtered molybdenum layer 2401, evaporated molybdenum layer 2402, sputtered molybdenum layer 2403 and cone 2426.

Referring back to Figure 23, as shown by step 2305, mask and etch steps are then performed. Figures 24E-24F show the structure of Figures 24C-24D after mask and etch steps have formed molybdenum structures 2430-2431 and an opening 2422 that extends to the top of lower electrode 4. In one embodiment, mask and etch step 2305 includes two separate mask and etch steps, a first mask and etch step that etches sputtered molybdenum layer 2403, evaporated molybdenum 2402 and molybdenum

layer 2401, and a second mask and etch step that etches through dielectric layer 6 and resistor layer 5 to form opening 2422.

Referring to step 2306 of Figure 23, a dielectric layer is deposited. In one embodiment, the dielectric layer is silicon dioxide.

Referring now to step 2307 of Figure 23, a passivation layer is deposited. In one embodiment, the passivation layer is silicon nitride deposited using a plasma enhanced chemical vapor deposition process. Figures 24G-24H show the structure of Figures 24E-34F after the deposition of dielectric layer 2440 and passivation layer 2441.

Referring now to step 2308, mask and etch steps are then performed. Referring now to Figures 24I-24J step 2308 forms openings 2450-2452 that extend through passivation layer 2441.

As shown in step 2309, Focusing structures are formed. A dry etch process is then performed as shown by step 2310. Referring now to Figures 24K-24L, steps 2309-2310 form polyimide focusing structures 2424 and openings 2461-2463 that extend through dielectric layer 2440. Opening 2462 extends to the top surface of lower contact pad 4, forming lower contact pad 2423. Referring now to Figure 24M, in the present embodiment, focus waffle metal 2427 is formed over focusing structures 2424.

Another etch is performed as shown by step 2311 to complete the structure. Referring now to Figures 24M-24N, etch step 2311 is shown to extend opening 2461 and opening 2463 of Figures 24K-24L through sputtered

molybdenum layer 2403 and evaporated molybdenum layer 2402, forming contact pad 2422 and removing that portion of sputtered molybdenum layer 2403 and evaporated molybdenum layer 2402 that overlie cone 2426.

In the process shown in Figures 23-24, dielectric layer 2440 and passivation layer 2441 protect upper electrodes 1810, preventing damage to upper electrode 1810 as typically occurs in prior art processes. By preventing damage to upper electrode 1810, upper electrode shorts and opens are prevented. In addition, because upper electrode 1810 is protected, column shorts in the frit seal region are eliminated. Also, because there is less exposed metal as compared with prior art processes, upper electrode to focus waffle shorts are decreased.

With reference now to Figures 25-26, yet another method for forming an electrode structure for a display device is shown. As shown by step 201 of Figure 25, lower electrodes are formed over a substrate. A resistor layer and a dielectric layer are then deposited over the lower electrodes as shown by steps 202-203. A gate metal layer is deposited as shown by step 204, followed by the formation of upper electrodes as shown by step 205. Mask and etch step 206 forms a gate structure. A cavity is then etched as shown by step 2301.

A layer of sputtered molybdenum, a layer of evaporated molybdenum, and a second layer of sputtered molybdenum are then deposited as shown by steps 2302-2304. In one embodiment, steps 201-206 and 2301-2304 are identical to steps 201-206 and 2301-2304 of Figure 23.

Referring now to step 2501 of Figure 25, a mask and etch step is performed that selectively etches both sputtered molybdenum layers and the evaporated molybdenum layer. In the present embodiment, mask and etch step 2501 removes all of that portion of the sputtered molybdenum layers and the evaporated molybdenum layers that overlie the region where the upper electrode contact pad is to be formed. That is, in the present embodiment, structure 2431 shown in figure 24F is also removed during etch step 2501.

Referring to step 2502 of Figure 25, a dielectric layer is deposited. In one embodiment, the dielectric layer is silicon dioxide.

Referring now to Figures 26A-26B, a substrate 1 is shown after steps 201-206, 2301-2304, and 2501-2502 of Figure 25 have formed dielectric layer 2600, molybdenum layer 2401, evaporated molybdenum layer 2402, and sputtered molybdenum layer 2403 such that cone 2426 is formed. Also shown are gate metal layer 1811 and upper electrodes 1810 that overlie dielectric layer 6, resistor layer 5 and lower electrode 4.

Referring now to step 2503 of Figure 25, mask and etch steps are performed. In one embodiment, mask and etch step 2503 includes three mask and etch steps, a first mask and etch step that produces the structure shown in Figures 26C-26D, a second mask and etch step that produces the structure shown in Figures 26E-26F and a third mask and etch step that produces the structure shown in Figures 26G-26H. Referring now to Figures 26G-26H, the third mask and etch step forms an opening that extends to lower electrode 4, forming contact pad 2643. In the present

embodiment, first and second etches are dry etches and the third etch is a wet etch. However, the present invention is well adapted to the use of different mask and etch processes for producing the structure shown in Figures 26G-26H.

As shown in step 2504, Focusing structures are formed. Referring to Figure 26I, in the present embodiment, focus waffle metal 2627 is formed over focusing structures 2624. As shown by step 2505 of Figure 25, an etch step is performed so as to further etch the remaining dielectric layer. In one embodiment, etch step 2504 uses a dry etch process. Referring now to Figures 26I-26J, step 2504 forms polyimide structures 2624 while step 2505 forms contact pad 2642.

Another etch is then performed as shown by step 2506 to complete the structure. In the present embodiment, as shown in Figures 26K-26L, etch step 2506 removes evaporated molybdenum layer 2553 and sputtered molybdenum layers 2552 and 2554.

Upper electrode 1810 is protected by dielectric layer 2600, preventing damage to upper electrode 1810 as typically occurs in prior art processes. By preventing damage to upper electrode 1810, upper electrode shorts and opens are prevented. In addition, because upper electrode 1810 is protected, column shorts in the frit seal region are eliminated. Also, because there is less exposed metal as compared with prior art processes, upper electrode to focus waffle shorts are decreased.

With reference now to Figures 27-28, yet another method for forming an electrode structure for a display device is shown. As shown by step 201 of Figure 27, lower electrodes are formed over a substrate. A resistor layer and a dielectric layer are then deposited over the lower electrodes as shown by steps 202-203. A gate metal layer is deposited as shown by step 204. Upper electrodes are then formed as shown by step 205. As shown by step 206, mask and etch steps are then performed to form a gate structure. Mask and etch steps are then performed as shown by step 2301 to form a cavity. In one embodiment, steps 201-206 and 2301 are identical to steps 201-206 and 2301 of Figure 23.

Continuing with Figure 27, a layer of evaporated chromium is then deposited as shown by step 2701, followed by the deposition of a layer of evaporated molybdenum as shown by step 2702. A dielectric layer is then deposited as shown by step 2703.

Referring to Figure 28A-28B, a substrate 1 is shown after steps 201-206 have formed lower electrodes 4, resistor layer 5, dielectric layer 6, gate metal structure 1811 and upper electrodes 1810. Etch step 2301 forms cavity 2425. Steps 2701-2703 result in the formation of evaporated chromium layer 2830, evaporated molybdenum layer 2831, and dielectric layer 2832.

Referring back to Figure 27, as shown by step 2704, mask and etch steps are then performed. Referring now to Figures 28C-28D, step 2704 etches through dielectric layer 2832, molybdenum layer 2831, evaporated chromium layer 2830 and partially etches upper electrodes 1810.

Continuing with Figure 27, as shown by step 2705, another etch step is performed that etches dielectric layer 6 and resistor layer 5, forming the structure shown in Figures 28E-28F. Step 2706 exposes a portion of lower electrode 4 so as to form contact pad 2823.

Continuing with Figure 27, as shown by step 2706, the focusing structure is formed. Referring now to Figures 28G-H, focusing structure 2824 is shown to be formed. Referring now to Figure 28G, in the present embodiment, focus waffle metal 2827 is formed over focusing structures 2824.

Continuing with Figure 27, as shown by step 2707, an etch step is performed. Referring now to Figures 28I-28J, step 2707 is shown to remove dielectric layer 2832 and to partially remove a portion of dielectric layer 6.

Another etch is then performed as shown by step 2708 to complete the structure. Figures 28K-28L show the structure of Figure 28I-28J after step 2708 has been performed. In the present embodiment, etch step 2708 removes evaporated molybdenum layer 2831.

During process steps 2704-2708, upper electrode 1810 is protected by evaporated chromium layer 2830. This prevents damage to upper electrode 1810 as typically occurs in prior art processes. By preventing damage to upper electrode 1810, upper electrode shorts and opens are prevented. In addition, because upper electrode 1810 is protected, column shorts in the frit seal region are eliminated. Also, because there is less exposed metal as compared with prior art processes, column to focus waffle shorts are decreased.

With reference now to Figures 29A-29H, side sectional views illustrating process steps used in the formation of a multilayer electrode and a side sectional view of a completed multilayer electrode for a flat panel display device is shown. The multilayer electrode of the present embodiment is suited for use, for example, as an electrode typically referred to as an upper electrode, a lower electrode, a gate electrode, a column electrode, a row electrode, or any other various type of electrode. Referring now to Figure 29A, in a starting step, a metal alloy layer 2902 is deposited above an underlying substrate 2900. In one embodiment, metal alloy layer 2902 is comprised of aluminum and neodymium which is deposited to a depth of approximately 2500 angstroms. The present invention is, however, well suited to embodiments which have a greater or lesser depth and/or to embodiments which are comprised of various other types of metal alloy layers.

With reference next to Figure 29B, after the formation of the structure of Figure 29A, the present embodiment deposits a protective layer 2904 above metal alloy layer 2902 to form a multilayer stack 2906. In one embodiment, protective layer 2904 is comprised of molybdenum and tungsten which is deposited to a depth of approximately 1200 angstroms. The present invention is, however, well suited to embodiments which have a greater or lesser depth and/or to embodiments which are comprised of various other types of protective layers.

As illustrated in Figure 29C, during normal process operations, contaminants, typically shown as 2908, are often deposited onto multilayer

stack 2906. Specifically, in some circumstances, watermarks contaminate the surface of multilayer stack 2906. Such contaminants can result in unwanted excess oxidation during subsequent etching operations. Such unwanted excess oxidation can jeopardize the controllability of subsequent etching operations and ultimately compromise the integrity of the resultant multilayer electrode. In fact, such compromising of the etching process can severely affect the formation of the electrode. In fact, "opens" or breaks in the multilayer electrode may result from unwanted excess oxidation and etching.

Referring now to Figure 29D, the present embodiment subjects multilayer stack 2906 to a cleansing process to remove oxidation-inducing contaminants 2908. In one embodiment, multilayer stack 2906 is subjected to a chemical solution to perform the cleansing process. Specifically, in one embodiment, the chemical solution used to perform the cleansing process is selected from the group consisting of NH_4OH, HF, and TMAH. As a result, the present embodiment provides a multilayer stack, shown in Figure 29D, which is substantially free of oxidation-inducing contaminants. Hence, the multilayer stack is not subjected, during subsequent etching operations, to the unwanted excess oxidation associated with conventional processes. Although the present embodiment specifically mentions the use of chemical solutions selected from the group consisting of NH_4OH, HF, and TMAH to perform the cleansing process, the present invention is also well suited to embodiments which utilize various other types of chemical solutions to perform the cleansing process.

Referring now to Figure 29E, after multilayer stack 2906 has been subjected to the above-described cleansing process, a layer of photoimagable material 2910 such as, for example, photoresist, is disposed above multilayer stack 2906. In the present embodiment, because multilayer stack 2906 has been subjected to the cleansing process, good adherence and topographical conformity is achieved between multilayer stack 2906 and layer of photoimagable material 2910. That is, unlike conventional processes in which the adherence and topographical conformity of the layer photoimagable material are compromised by underlying contaminants, the present embodiment is substantially free of such defects.

With reference now to Figure 29F, multilayer stack 2906 is shown having only a remaining portion of layer of photoimagable material 2910 disposed thereon. More specifically, the structure of Figure 29F is obtained after a masking and photoimagable material removal process has been performed on the structure of Figure 29E.

Referring next to Figure 29G, multilayer stack 2906 is shown after the structure of Figure 29F has been subjected to an etching process. As shown in Figure 29G, the region of multilayer stack 2906 which resides beneath remaining portion of layer of photoimagable material 2910 is protected from the etching process. That is, the bulk of the etching occurs to that portion of multilayer stack 2906 which does not have the remaining portion of layer of photoimagable material 2910 disposed thereover. In the present embodiment, the etching process is performed using a wet etching of multilayer stack 2906. More specifically, in the present embodiment, a wet etching of multilayer stack 2906 is performed with a wet etchant

comprised of H_3PO_4, HNO_3, CH_3COOH, and H_2O. In this embodiment, the volume percentages of the wet etchant constituents are as follows: approximately 70-80 percent H_3PO_4; approximately 10-15 percent HNO_3; approximately 7-12 percent CH_3COOH; and approximately 2-8 percent H_2O. Although the present embodiment specifically mentions the use of a wet etchant comprised of the aforementioned volume percentages of H_3PO_4, HNO_3, CH_3COOH, and H_2O to perform the etching process, the present invention is also well suited to embodiments which utilize various other volume percentages and/or to the use of various other types of wet etchants to perform the etching process.

Referring still to Figure 29G, in the present embodiment, the etching process is comprised of two portions. More specifically, the wet etchant of H_3PO_4, HNO_3, CH_3COOH, and H_2O first causes an oxidation of multilayer stack 2906, and then proceeds to etch the oxidized region of multilayer stack 2906. In the present embodiment, the HNO_3 constituent of the wet etchant is largely responsible for the oxidation of multilayer stack 2906. The H_3PO_4 and CH_3COOH constituents of the wet etchant are largely responsible for the etching of the oxidized portion of multilayer stack 2906. As mentioned above, the present embodiment provides a multilayer stack, shown in Figure 29D, which is substantially free of oxidation-inducing contaminants. Hence, multilayer stack 2906 is not subjected, during the etching operation using H_3PO_4, HNO_3, CH_3COOH, and H_2O, to the unwanted excess oxidation associated with conventional processes. Thus, in the present embodiment, multilayer stack 2906 is both predictably and controllably oxidized and subsequently etched. As a result, the multilayer electrode created by the present embodiment is not subject to the "opens" or

breaks found in conventional multilayer electrodes which have been subjected to unwanted excess oxidation and etching.

Furthermore in the present embodiment, the use of the above-described multilayer stack 2906 has significant advantages associated therewith. As one example, the etch rates of the two layers (i.e. the molybdenum/tungsten layer and the aluminum/neodymium layer) and the respective depths of the two layers provide a structure which etches in a manner to provide an ideal sloped-edge profile for the completed multilayer electrode.

Referring now to Figure 29H, a side sectional view of a completed multilayer electrode 2912 is shown. Due to the aforementioned cleansing operation and the use of the above-described wet etchant, completed multilayer electrode 2912 has an excellent taper angle; does not suffer from a ragged etch profile; has good wet etch uniformity; and does not suffer from the "opens" or breaks found in conventional multilayer electrodes.

With reference now to Figure 30, a flow chart reciting steps associated with the formation of a multilayer electrode in accordance with one embodiment of the present claimed invention is shown.

As is described above in detail, at step 3002, the present embodiment deposits a metal alloy layer.

At step 3004, subsequent to the deposition of the metal alloy layer, a protective layer is deposited above the metal alloy layer to form a multilayer stack.

At step 3006, the present embodiment subjects the multilayer stack to a cleansing process to remove excess oxidation-inducing contaminants.

At step 3008, the present embodiment etches the cleansed multilayer stack to form a multilayer electrode.

Thus, the present invention provides, in this embodiment, a multilayer electrode and a method of forming such a multilayer electrode wherein the multilayer stack from which the multilayer electrode is formed is not subjected to unwanted excess oxidation during the electrode formation process. The present embodiment further provides a multilayer electrode and a method of forming such a multilayer electrode wherein the multilayer electrode does not suffer from excessive "opens" or breaks.

With reference now to Figures 31A-31I, side sectional views illustrating process steps used in the formation of a multilayer electrode with reduced formation of an intermetallic compound and a side sectional view of a completed multilayer electrode with reduced formation of an intermetallic compound for a flat panel display device is shown. The multilayer electrode of the present embodiment is suited for use, for example, as an electrode typically referred to as an upper electrode, a lower electrode, a gate electrode, a column electrode, a row electrode, or any other various type of electrode. Referring now to Figure 31A, in a starting step, a

first metal alloy layer 3102 is deposited above an underlying substrate 3100. In one embodiment, metal alloy layer 3102 is comprised of aluminum and neodymium which is deposited to a depth of approximately 2500 angstroms. The present invention is, however, well suited to embodiments which have a greater or lesser depth and/or to embodiments which are comprised of various other types of metal alloy layers.

Referring still to Figure 31A, in the present embodiment, the deposition of first metal alloy layer 3102 is performed in a vacuum environment. Such a vacuum environment is typically maintained at, for example, approximately 1-5 milliTorr. In conventional operations, the second metal alloy layer (also referred to in herein as a protective layer) is then deposited above the first metal alloy layer within the same vacuum environment.

With reference next to Figure 31B, after the formation of the structure of Figure 31A, the present embodiment forms a barrier layer 3103 above the first metal layer 3102. Barrier layer 3101 of the present embodiment is adapted to prevent the formation of an intermetallic compound within first metal alloy layer 3102. In the present embodiment, barrier layer 3103 is formed by subjecting first metal alloy layer 3102 to an oxygen containing environment such that a native oxide layer is formed on first metal alloy layer 3102. More specifically, in one embodiment, the oxygen containing environment is obtained by breaking the vacuum environment utilized during the deposition of first metal alloy layer 3102 and allowing air to contact first metal alloy layer 3102. In one embodiment, the previously evacuated environment in which the deposition of the first

metal alloy layer 3102 took place is brought to approximately atmospheric pressure (one atmosphere), and is filled with air. In so doing, oxygen in the air reacts with the surface of first metal alloy layer 3102 such that a native oxide layer is formed. In one embodiment, the native oxide layer is formed having a thickness of less than approximately 100 angstroms. Although the present embodiment specifically mentions the use of air and a pressure of approximately one atmosphere, the present invention is also well suited to embodiments which utilize various other oxygen containing gases and/or to the use of various other pressures to perform the barrier layer formation process.

With reference still to Figure 31B, in still another embodiment, the present embodiment forms barrier layer 3103 by introducing oxygen into the environment utilized during the deposition of first metal alloy layer 3102. Specifically, in one embodiment, oxygen is introduced into the environment utilized during the deposition of first metal alloy layer 3102 at a rate of approximately 1-5 sccm (standard cubic centimeters per minute). Although the present embodiment specifically mentions the use of air and flow rate of approximately 1-5 sccm, the present invention is also well suited to embodiments which utilize various other oxygen containing gases and/or to the use of various other flow rates to perform the barrier layer formation process.

Referring yet again to Figure 31B, in one embodiment, the present invention subjects a target material to be subsequently used in the deposition of a second metal alloy layer (not shown in Figure 31B) to a pre-sputter cleansing process. This process is intended to clean the target of

any oxidation or other unwanted contamination which may be present after the deposition of first metal alloy layer 3102 and the formation of barrier layer 3103.

Referring now to Figure 31C, the present embodiment then deposits a second metal alloy layer (also referred to above as a protective layer) 3104 above first metal alloy layer 3102 to form a multilayer stack 3106. In one embodiment, protective layer 3104 is comprised of molybdenum and tungsten which is deposited to a depth of approximately 1200 angstroms. The present invention is, however, well suited to embodiments which have a greater or lesser depth and/or to embodiments which are comprised of various other types of protective layers.

With reference still to Figure 31C, barrier layer 3103 prevents the formation of an intermetallic compound within second metal alloy layer 3104. That is, barrier layer 3103 prevents the atoms and molecules of the two separate metal layers (i.e. first metal alloy layer 3102 and second metal alloy layer 3104) from diffusing to form a new compound. Thus, unlike prior art processes, the present embodiment does not suffer from significant formation of intermetallic compounds during the electrode formation process. Hence, the oxidation and etch rates of the multilayer stack formed by the present method are well known. As a result, the multilayer stack of the present embodiment does not suffer from the variation and unpredictability in subsequent oxidation and etching processes as is found in the prior art. Multilayer stack 3106 is now well suited to being formed into a multilayer electrode for use, for example, in a flat panel display device.

Figures 31D-31I depict additional steps performed in accordance with one embodiment of the present invention in which a cleansing operation is performed prior to etching of multilayer stack 3106 to form the multilayer electrode. As illustrated in Figure 31D, during normal process operations, contaminants, typically shown as 3108, are often deposited onto multilayer stack 3106. Specifically, in some circumstances, watermarks contaminate the surface of multilayer stack 3106. Such contaminants can result in unwanted excess oxidation during subsequent etching operations. Such unwanted excess oxidation can jeopardize the controllability of subsequent etching operations and ultimately compromise the integrity of the resultant multilayer electrode. In fact, such compromising of the etching process can severely affect the formation of the electrode. In fact, "opens" or breaks in the multilayer electrode may result from unwanted excess oxidation and etching.

Referring now to Figure 31E, the present embodiment subjects multilayer stack 3106 to a cleansing process to remove oxidation-inducing contaminants 3108. In one embodiment, multilayer stack 3106 is subjected to a chemical solution to perform the cleansing process. Specifically, in one embodiment, the chemical solution used to perform the cleansing process is selected from the group consisting of NH_4OH, HF, and TMAH. As a result, the present embodiment provides a multilayer stack, shown in Figure 31E, which is substantially free of oxidation-inducing contaminants. Hence, the multilayer stack is not subjected, during subsequent etching operations, to the unwanted excess oxidation associated with conventional processes. Although the present embodiment specifically mentions the use

of chemical solutions selected from the group consisting of NH_4OH, HF, and TMAH to perform the cleansing process, the present invention is also well suited to embodiments which utilize various other types of chemical solutions to perform the cleansing process.

Referring now to Figure 31F, after multilayer stack 3106 has been subjected to the above-described cleansing process, a layer of photoimagable material 3110 such as, for example, photoresist, is disposed above multilayer stack 3106. In the present embodiment, because multilayer stack 3106 has been subjected to the cleansing process, good adherence and topographical conformity is achieved between multilayer stack 3106 and layer of photoimagable material 3110. That is, unlike conventional processes in which the adherence and topographical conformity of the layer photoimagable material are compromised by underlying contaminants, the present embodiment is substantially free of such defects.

With reference now to Figure 31G, multilayer stack 3106 is shown having only a remaining portion of layer of photoimagable material 3110 disposed thereon. More specifically, the structure of Figure 31G is obtained after a masking and photoimagable material removal process has been performed on the structure of Figure 31F.

Referring next to Figure 31H, multilayer stack 3106 is shown after the structure of Figure 31G has been subjected to an etching process. As shown in Figure 31H, the region of multilayer stack 3106 which resides beneath remaining portion of layer of photoimagable material 3110 is protected from the etching process. That is, the bulk of the etching occurs

to that portion of multilayer stack 3106 which does not have the remaining portion of layer of photoimagable material 3110 disposed thereover. In the present embodiment, the etching process is performed using a wet etching of multilayer stack 3106. More specifically, in the present embodiment, a wet etching of multilayer stack 3106 is performed with a wet etchant comprised of H_3PO_4, HNO_3, CH_3COOH, and H_2O. In this embodiment, the volume percentages of the wet etchant constituents are as follows: approximately 70-80 percent H_3PO_4; approximately 10-15 percent HNO_3; approximately 7-12 percent CH_3COOH; and approximately 2-8 percent H_2O. Although the present embodiment specifically mentions the use of a wet etchant comprised of the aforementioned volume percentages of H_3PO_4, HNO_3, CH_3COOH, and H_2O to perform the etching process, the present invention is also well suited to embodiments which utilize various other volume percentages and/or to the use of various other types of wet etchants to perform the etching process.

Referring still to Figure 31H, in the present embodiment, the etching process is comprised of two portions. More specifically, the wet etchant of H_3PO_4, HNO_3, CH_3COOH, and H_2O first causes an oxidation of multilayer stack 3106, and then proceeds to etch the oxidized region of multilayer stack 3106. In the present embodiment, the HNO_3 constituent of the wet etchant is largely responsible for the oxidation of multilayer stack 3106. The H_3PO_4 and CH_3COOH constituents of the wet etchant are largely responsible for the etching of the oxidized portion of multilayer stack 3106. As mentioned above, the present embodiment provides a multilayer stack, shown in Figure 31E, which is substantially free of oxidation-inducing contaminants. Hence, multilayer stack 3106 is not subjected, during the etching operation

using H_3PO_4, HNO_3, CH_3COOH, and H_2O, to the unwanted excess oxidation associated with conventional processes. Thus, in the present embodiment, multilayer stack 3106 is both predictably and controllably oxidized and subsequently etched. As a result, the multilayer electrode created by the present embodiment is not subject to the "opens" or breaks found in conventional multilayer electrodes which have been subjected to unwanted excess oxidation and etching.

Furthermore in the present embodiment, the use of the above-described multilayer stack 3106 has significant advantages associated therewith. As one example, the etch rates of the two layers (i.e. the molybdenum/tungsten layer and the aluminum/neodymium layer) and the respective depths of the two layers provide a structure which etches in a manner to provide an ideal sloped-edge profile for the completed multilayer electrode.

Referring now to Figure 31I, a side sectional view of a completed multilayer electrode 3112 is shown. Due to the aforementioned cleansing operation and the use of the above-described wet etchant, completed multilayer electrode 3112 has an excellent taper angle; does not suffer from a ragged etch profile; has good wet etch uniformity; and does not suffer from the "opens" or breaks found in conventional multilayer electrodes.

With reference now to Figure 32, a flow chart reciting steps associated with the formation of a multilayer electrode with reduced intermetallic compound formation in accordance with one embodiment of the present claimed invention is shown.

As is described above in detail, at step 3202, the present embodiment deposits a first metal alloy layer.

At step 3203, subsequent to the deposition of the first metal alloy layer and prior to the deposition of a second metal alloy layer, a barrier layer is formed above the first metal alloy layer.

At step 3204, subsequent to the formation of the barrier layer, a second metal alloy layer (also referred to as a protective layer) is deposited above the barrier layer to form a multilayer stack. The barrier layer prevents the formation of intermetallic compounds between the first metal alloy layer and the second metal alloy layer.

At step 3206, the present embodiment subjects the multilayer stack to a cleansing process to remove excess oxidation-inducing contaminants.

At step 3208, the present embodiment etches the cleansed multilayer stack to form a multilayer electrode.

Thus, the present invention provides a multilayer electrode and a method of forming such a multilayer electrode wherein the multilayer stack, from which the multilayer electrode is formed, does not suffer from significant formation of intermetallic compounds during the electrode formation process.

The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the Claims appended hereto and their equivalents.

CLAIMS

1. A method for forming a multilayer electrode for a flat panel display device, said method comprising the steps of:

a) depositing a metal alloy layer;

b) depositing a protective layer above said metal alloy layer to form a multilayer stack;

c) subjecting said multilayer stack to a cleansing process to remove contaminants; and

d) etching said multilayer stack to form said multilayer electrode for said flat panel display device.

2. The method for forming a multilayer electrode for a flat panel display device as recited in Claim 1, wherein step a) comprises depositing a metal alloy layer of aluminum and neodymium.

3. The method for forming a multilayer electrode for a flat panel display device as recited in Claim 1, wherein step a) comprises depositing said metal alloy layer to a depth of approximately 2500 angstroms.

4. The method for forming a multilayer electrode for a flat panel display device as recited in Claim 1, wherein step b) comprises depositing a protective layer comprised of molybdenum and tungsten.

5. The method for forming a multilayer electrode for a flat panel display device as recited in Claim 1, wherein step b) comprises depositing said protective layer to a depth of approximately 1200 angstroms

6. The method for forming a multilayer electrode for a flat panel display device as recited in Claim 1, wherein step c) comprises subjecting said multilayer stack to a chemical solution.

7. The method for forming a multilayer electrode for a flat panel display device as recited in Claim 6, wherein said chemical solution is selected from the group consisting of NH_4OH, HF, and TMAH.

8. The method for forming a multilayer electrode for a flat panel display device as recited in Claim 1, wherein step d) comprises wet etching said multilayer stack to form said multilayer electrode for said flat panel display device.

9. The method for forming a multilayer electrode for a flat panel display device as recited in Claim 7, wherein step d) comprises wet etching said multilayer stack with a wet etchant comprised of H_3PO_4, HNO_3, CH_3COOH, and H_2O to form said multilayer electrode for said flat panel display device.

10. A method for cleansing and etching a multilayer stack during the formation of a multilayer electrode for a flat panel display device, said method comprising the steps of:

a) subjecting said multilayer stack to a cleansing process to remove oxidation-inducing contaminants such that unwanted excess oxidation caused by said oxidation-inducing contaminants is reduced; and

b) etching said multilayer stack, cleansed in step a), to form said multilayer electrode for said flat panel display device.

11. The method for cleansing and etching a multilayer stack during the formation of a multilayer electrode for a flat panel display device as recited in Claim 10, wherein said multilayer layer stack is comprised of a metal alloy layer and a protective layer.

12. The method for cleansing and etching a multilayer stack during the formation of a multilayer electrode for a flat panel display device as recited in Claim 11, wherein said metal alloy layer is comprised of aluminum and neodymium.

13. The method for cleansing and etching a multilayer stack during the formation of a multilayer electrode for a flat panel display device as recited in Claim 11, wherein said metal alloy layer is deposited to a depth of approximately 2500 angstroms.

14. The method for cleansing and etching a multilayer stack during the formation of a multilayer electrode for a flat panel display device as recited in Claim 11, wherein said protective layer is comprised of molybdenum and tungsten.

15. The method for cleansing and etching a multilayer stack during the formation of a multilayer electrode for a flat panel display device as recited in Claim 11, wherein said protective layer is deposited to a depth of approximately 1200 angstroms.

16. The method for cleansing and etching a multilayer stack during the formation of a multilayer electrode for a flat panel display device as recited in Claim 11, wherein step a) comprises subjecting said multilayer stack to a chemical solution.

17. The method for cleansing and etching a multilayer stack during the formation of a multilayer electrode for a flat panel display device as recited in Claim 16, wherein said chemical solution is selected from the group consisting of NH_4OH, HF, and TMAH.

18. The method for cleansing and etching a multilayer stack during the formation of a multilayer electrode for a flat panel display device as recited in Claim 11, wherein step b) comprises wet etching said multilayer stack to form said multilayer electrode for said flat panel display device.

19. The method for cleansing and etching a multilayer stack during the formation of a multilayer electrode for a flat panel display device as recited in Claim 11, wherein step b) comprises wet etching said multilayer stack with a wet etchant comprised of H_3PO_4, HNO_3, CH_3COOH, and H_2O to form said multilayer electrode for said flat panel display device.

20. A multilayer electrode for a flat panel display device, said multilayer electrode comprising:

a metal alloy layer; and

a protective layer disposed above said metal alloy layer to form a multilayer stack, said multilayer stack etched to form said multilayer electrode.

21. The multilayer electrode for a flat panel display device as recited in Claim 20, wherein said metal alloy layer is comprised of aluminum and neodymium.

22. The multilayer electrode for a flat panel display device as recited in Claim 20, wherein said metal alloy layer has a depth of approximately 2500 angstroms.

23. The multilayer electrode for a flat panel display device as recited in Claim 20, wherein said protective layer is comprised of molybdenum and tungsten.

24. The multilayer electrode for a flat panel display device as recited in Claim 20, wherein said protective layer has a depth of approximately 1200 angstroms.

25. A method for forming a multilayer stack with reduced formation of an intermetallic compound, said method comprising the steps of:

a) depositing a first metal alloy layer above a substrate;

b) forming a barrier layer above said first metal alloy layer, said barrier layer adapted to prevent the formation of an intermetallic compound within said first metal alloy layer; and

c) depositing a second metal alloy layer above said barrier layer, said barrier layer preventing the formation of said intermetallic compound within said second metal alloy layer.

26. The method for forming a multilayer stack with reduced formation of an intermetallic compound as recited in Claim 25, wherein step a) comprises depositing a first metal alloy layer of aluminum and neodymium above said substrate.

27. The method for forming a multilayer stack with reduced formation of an intermetallic compound as recited in Claim 25, wherein step a) comprises depositing said first metal alloy layer to a depth of approximately 2500 angstroms.

28. The method for forming a multilayer stack with reduced formation of an intermetallic compound as recited in Claim 25, wherein step b) comprises forming said barrier layer by subjecting said first metal alloy layer to an oxygen containing environment such that a native oxide layer is formed on said first metal alloy layer.

29. The method for forming a multilayer stack with reduced intermetallic compounds as recited in Claim 28, wherein said oxygen containing environment is obtained by breaking a vacuum utilized during said deposition of said first metal alloy layer and allowing air to contact said first metal alloy layer.

30. The method for forming a multilayer stack with reduced intermetallic compounds as recited in Claim 28, wherein said oxygen containing environment is obtained by introducing oxygen into an environment utilized during said deposition of said first metal alloy layer.

31. The method for forming a multilayer stack with reduced intermetallic compounds as recited in Claim 25 further comprising the step of:

after step b) and prior to step c), subjecting a target material used in the deposition of said second metal alloy layer to a pre-sputter cleansing process.

32. The method for forming a multilayer stack with reduced intermetallic compounds as recited in Claim 25, wherein step c) comprises depositing a second metal alloy layer comprised of molybdenum and tungsten above said barrier layer.

33. The method for forming a multilayer stack with reduced intermetallic compounds as recited in Claim 25, wherein step c) comprises depositing said second metal alloy layer to a depth of approximately 1200 angstroms.

34. A method for forming a multilayer electrode for a flat panel display device, wherein said method reduces the formation of an intermetallic compound during the fabrication of said multilayer electrode, said method comprising the steps of:

a) depositing a first metal alloy layer above a substrate;

b) forming a barrier layer above said first metal alloy layer, said barrier layer adapted to prevent the formation of an intermetallic compound within said first metal alloy layer;

c) depositing a second metal alloy layer above said barrier layer to form a multilayer stack, said barrier layer preventing the formation of said intermetallic compound within said second metal alloy layer;

d) subjecting said multilayer stack to a cleansing process to remove contaminants; and

e) etching said multilayer stack to form said multilayer electrode for said flat panel display device.

35. The method for forming a multilayer electrode for a flat panel display device as recited in Claim 34, wherein step a) comprises depositing a first metal alloy layer of aluminum and neodymium above said substrate.

36. The method for forming a multilayer electrode for a flat panel display device as recited in Claim 34, wherein step a) comprises depositing said first metal alloy layer to a depth of approximately 2500 angstroms.

37. The method for forming a multilayer electrode for a flat panel display device as recited in Claim 34, wherein step b) comprises forming said barrier layer by subjecting said first metal alloy layer to an oxygen containing environment such that a native oxide layer is formed on said first metal alloy layer.

38. The method for forming a multilayer electrode for a flat panel display device as recited in Claim 37, wherein said oxygen containing environment is obtained by breaking a vacuum utilized during said deposition of said first metal alloy layer and allowing air to contact said first metal alloy layer.

39. The method for forming a multilayer electrode for a flat panel display device as recited in Claim 37, wherein said oxygen containing environment is obtained by introducing oxygen into an environment utilized during said deposition of said first metal alloy layer.

40. The method for forming a multilayer electrode for a flat panel display device as recited in Claim 34 further comprising the step of:

after step b) and prior to step c), subjecting a target material used in the deposition of said second metal alloy layer to a pre-sputter cleansing process.

41. The method for forming a multilayer electrode for a flat panel display device as recited in Claim 34, wherein step c) comprises depositing a second metal alloy layer comprised of molybdenum and tungsten above said barrier layer.

42. The method for forming a multilayer electrode for a flat panel display device as recited in Claim 34, wherein step c) comprises depositing said second metal alloy layer to a depth of approximately 1200 angstroms.

43. The method for forming a multilayer electrode for a flat panel display device as recited in Claim 34, wherein step d) comprises subjecting said multilayer stack to a chemical solution prior to deposition of a photoresist layer.

44. The method for forming a multilayer electrode for a flat panel display device as recited in Claim 43, wherein said chemical solution is selected from the group consisting of NH_4OH, HF, and TMAH.

45. The method for forming a multilayer electrode for a flat panel display device as recited in Claim 34, wherein step e) comprises wet etching said multilayer stack to form said multilayer electrode for said flat panel display device.

46. The method for forming a multilayer electrode for a flat panel display device as recited in Claim 34, wherein step e) comprises wet etching said multilayer stack with a wet etchant comprised of H_3PO_4, HNO_3, CH_3COOH, and H_2O to form said multilayer electrode for said flat panel display device.

47. A multilayer electrode for a flat panel display device, said multilayer electrode comprising:

a metal alloy layer;

a barrier layer disposed above said metal alloy layer; and

a protective layer disposed above said barrier layer to form a multilayer stack, said multilayer stack etched to form said multilayer electrode.

48. The multilayer electrode for a flat panel display device as recited in Claim 47, wherein said metal alloy layer is comprised of aluminum and neodymium.

49. The multilayer electrode for a flat panel display device as recited in Claim 47, wherein said metal alloy layer has a depth of approximately 2500 angstroms.

50. The multilayer electrode for a flat panel display device as recited in Claim 47, wherein said barrier layer is comprised of a native oxide layer of said metal alloy layer.

51. The multilayer electrode for a flat panel display device as recited in Claim 47, wherein said barrier layer has a depth of less than approximately 100 angstroms.

52. The multilayer electrode for a flat panel display device as recited in Claim 47, wherein said protective layer is comprised of molybdenum and tungsten.

53. The multilayer electrode for a flat panel display device as recited in Claim 47, wherein said protective layer has a depth of approximately 1200 angstroms.

54. The multilayer electrode for a flat panel display device as recited in Claim 47, wherein said multilayer electrode is etched using a wet etchant with volume percentages of constituents of approximately 70-80 percent H_3PO_4; approximately 10-15 percent HNO_3; approximately 7-12 percent CH_3COOH; and approximately 2-8 percent H_2O to form a desired sloped profile.

MULTILAYER ELECTRODE STRUCTURE AND METHOD FOR FORMING MULTILAYER ELECTRODE STRUCTURE FOR A FLAT PANEL DISPLAY DEVICE

ABSTRACT OF THE DISCLOSURE

A multilayer electrode for a flat panel display device and a method for forming a multilayer electrode for a flat panel display device. In one embodiment, the multilayer electrode is formed by depositing a metal alloy layer. After the deposition of the metal alloy layer, the present embodiment deposits a protective layer above the metal alloy layer to form a multilayer stack. The present embodiment then subjects the multilayer stack to a cleansing process to remove contaminants. Subsequently, the present embodiment etches the multilayer stack to form the multilayer electrode for the flat panel display device. In another embodiment, the present invention provides a method for forming a multilayer stack with reduced formation of an intermetallic compound. In such an embodiment, the present embodiment deposits a first metal alloy layer above a substrate. Next, the present embodiment forms a barrier layer above the first metal alloy layer. In this embodiment, the barrier layer is adapted to prevent the formation of an intermetallic compound within the first metal alloy layer. Next, the present embodiment deposits a second metal alloy layer above the barrier layer. In so doing, the barrier layer also prevents the formation of the intermetallic compound within the second metal alloy layer.

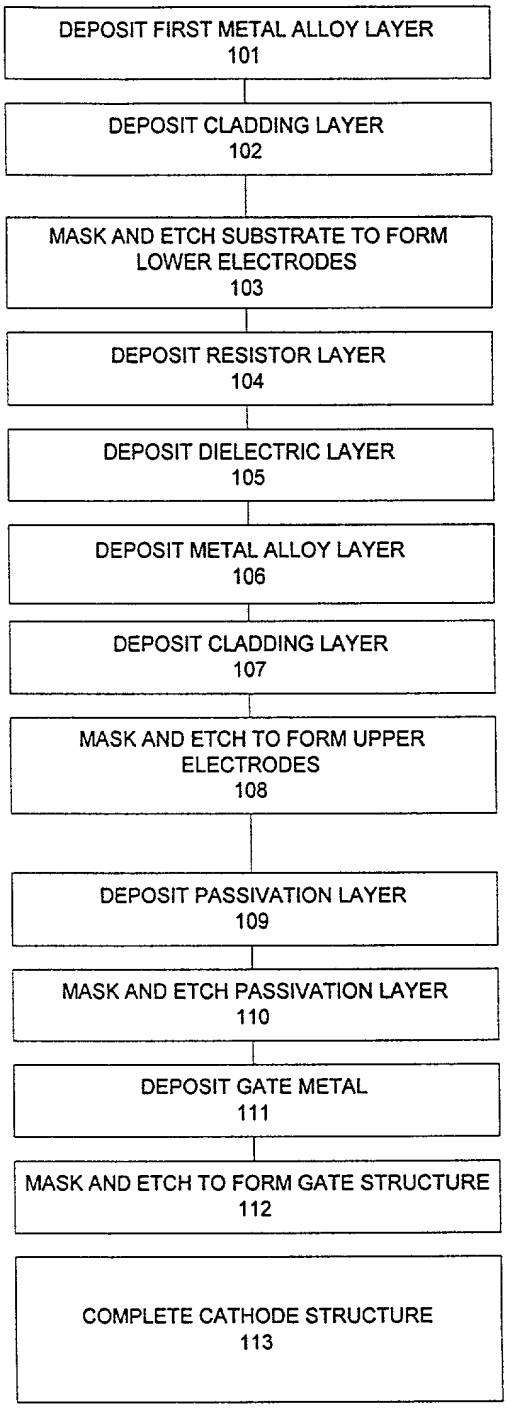

DEPOSIT FIRST METAL ALLOY LAYER
101
DEPOSIT CLADDING LAYER
102
MASK AND ETCH SUBSTRATE TO FORM LOWER ELECTRODES
103
DEPOSIT RESISTOR LAYER
104
DEPOSIT DIELECTRIC LAYER
105
DEPOSIT METAL ALLOY LAYER
106
DEPOSIT CLADDING LAYER
107
MASK AND ETCH TO FORM UPPER ELECTRODES
108
DEPOSIT PASSIVATION LAYER
109
MASK AND ETCH PASSIVATION LAYER
110
DEPOSIT GATE METAL
111
MASK AND ETCH TO FORM GATE STRUCTURE
112
COMPLETE CATHODE STRUCTURE
113

FIG. 1

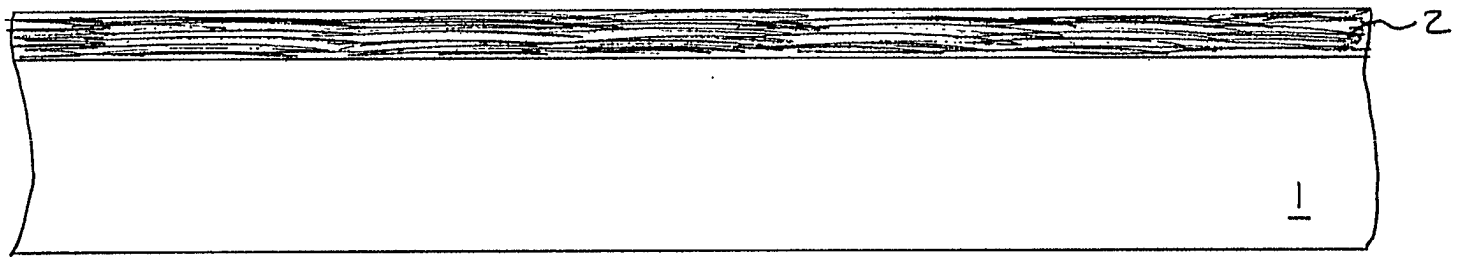


FIG. 2

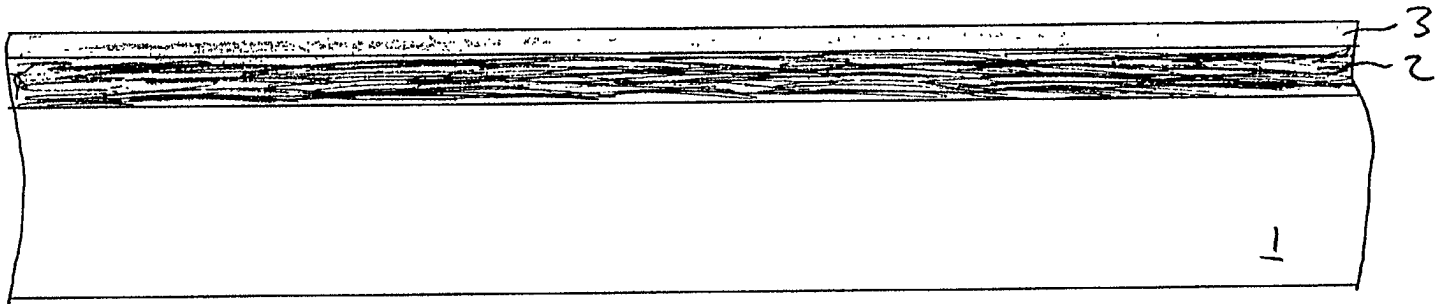


FIG. 3

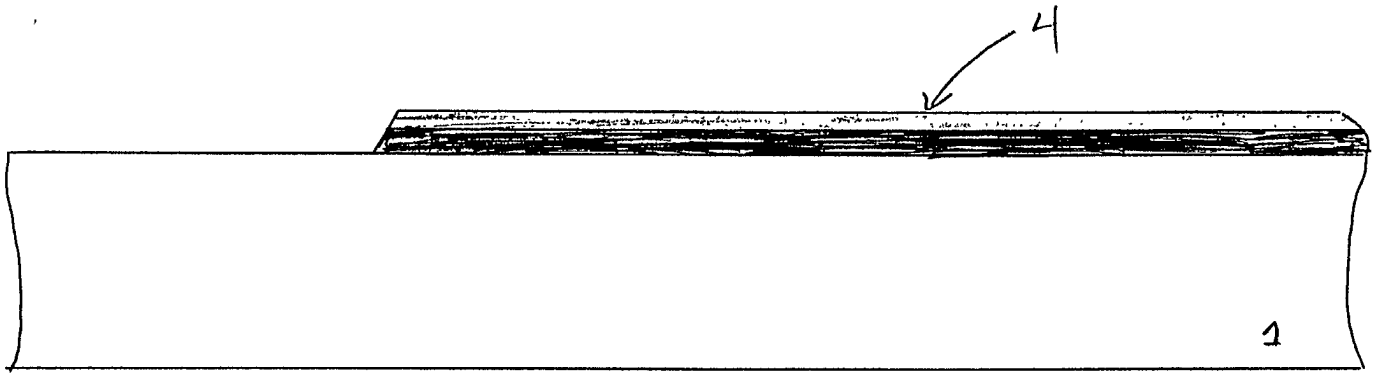


FIG. 4A

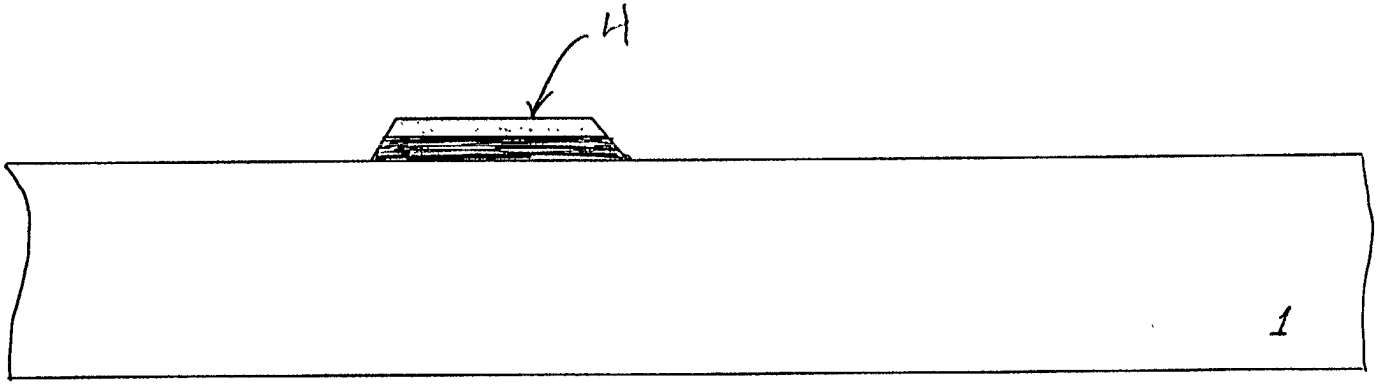


FIG. 4B

FIG. 5A

FIG. 5B

FIG. 6A

FIG. 6B

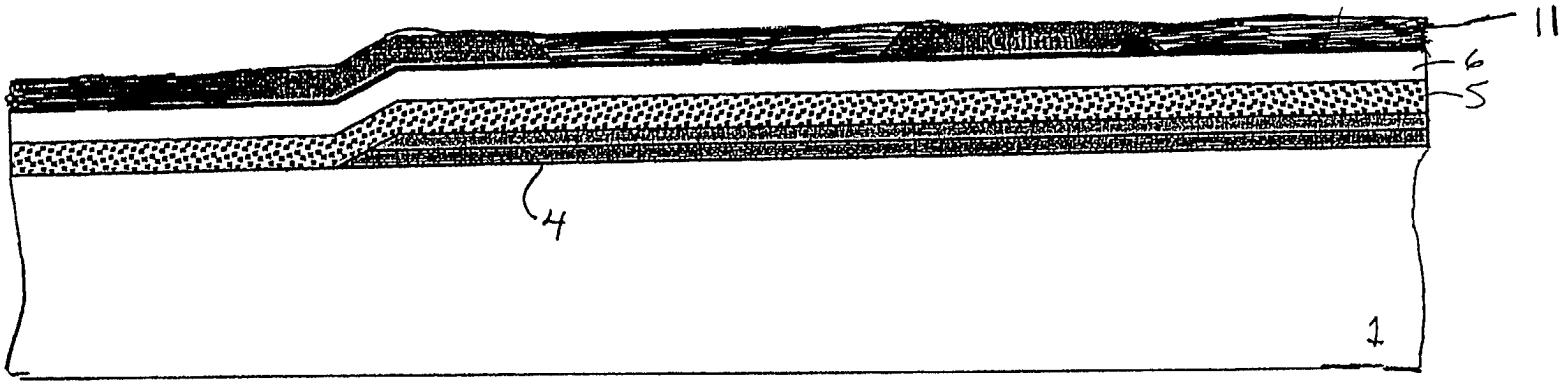


FIG. 7A

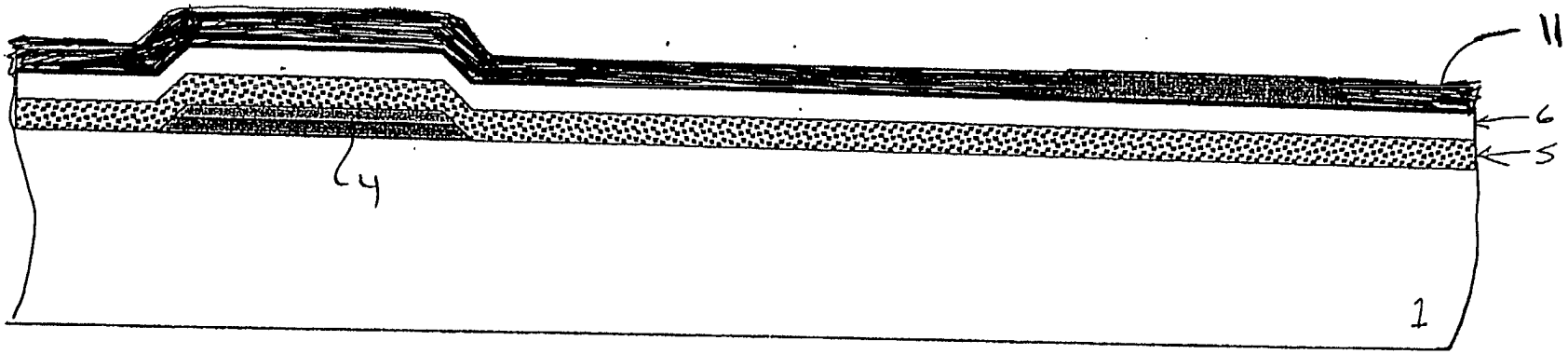
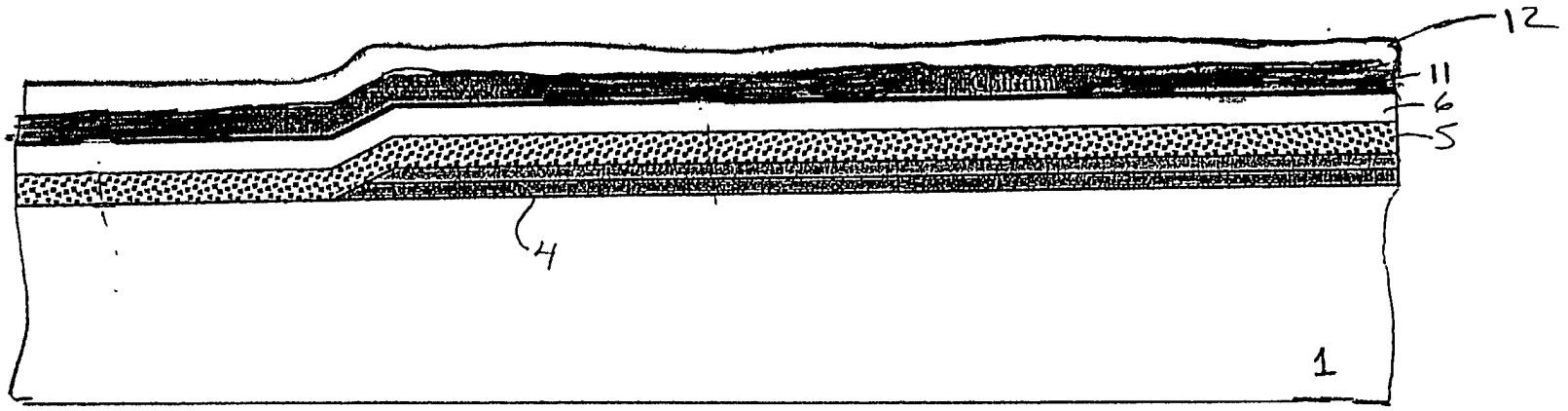


FIG. 7B



FIG, 8A

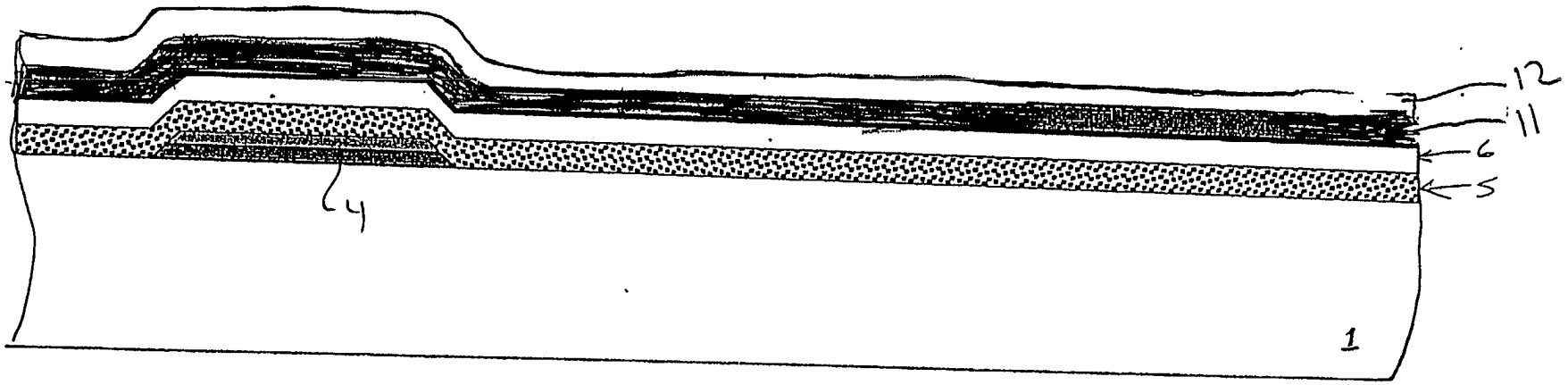


FIG. 8B

FIG. 9A

FIG. 9B

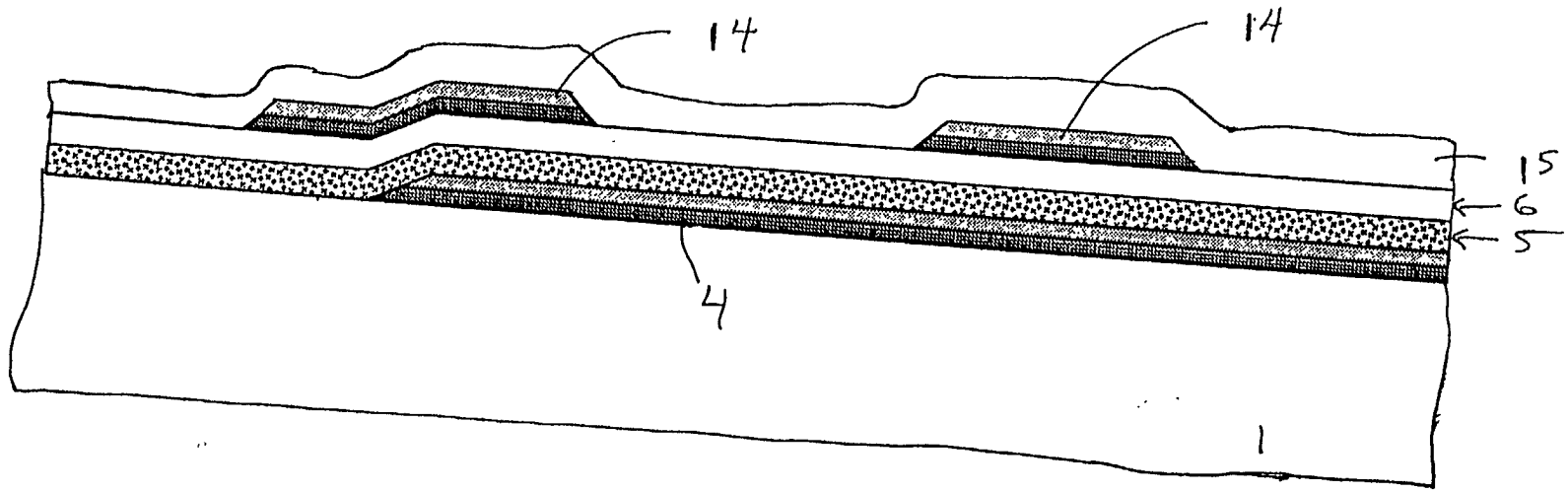


FIG. 10A

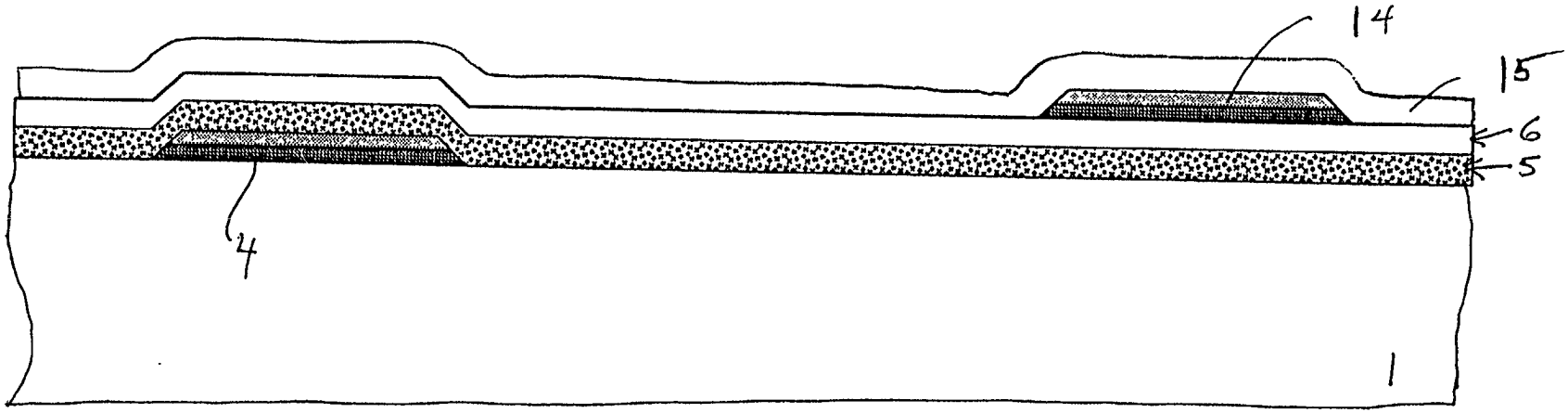


FIG. 10B

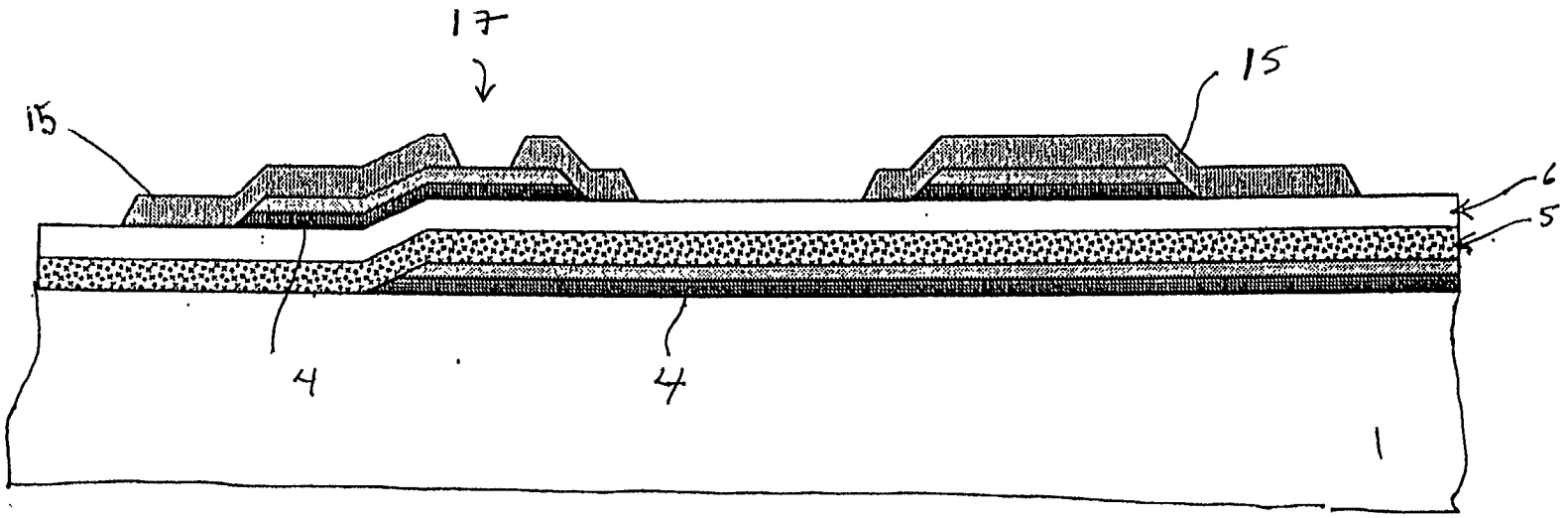


FIG. 11A

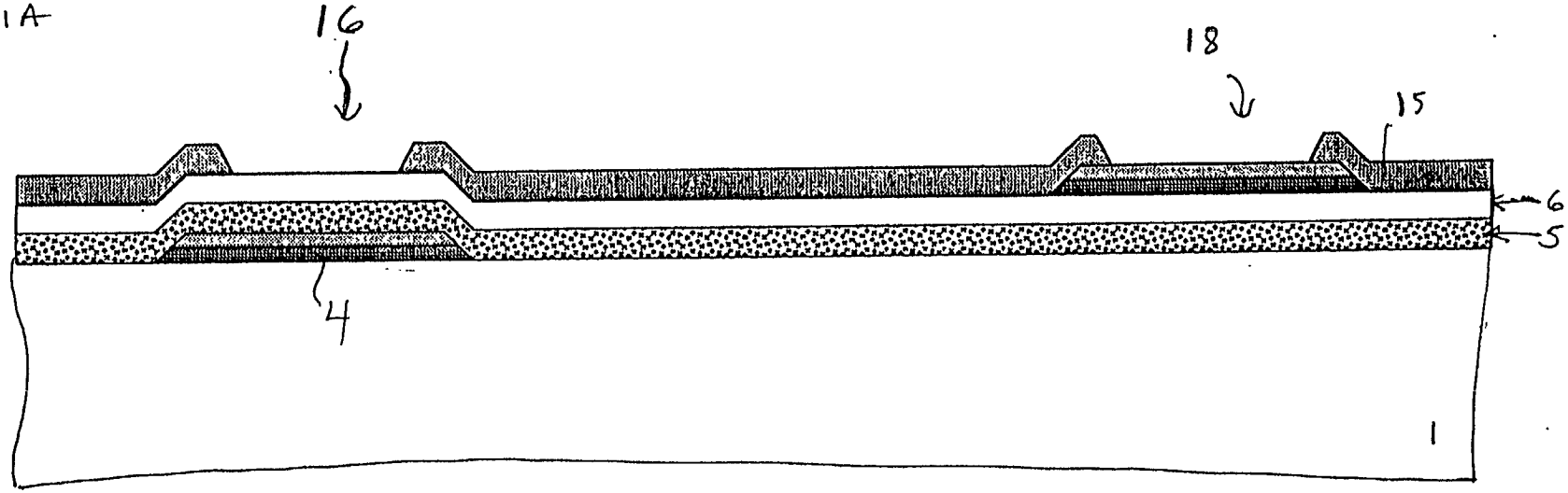


FIG. 11B

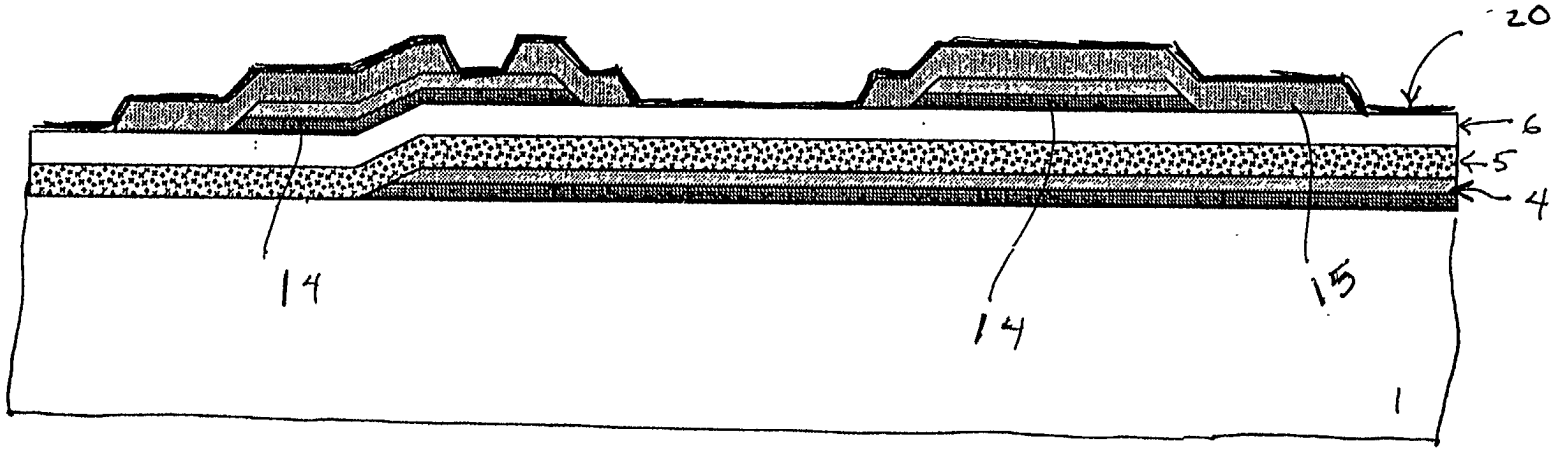


FIG. 12A

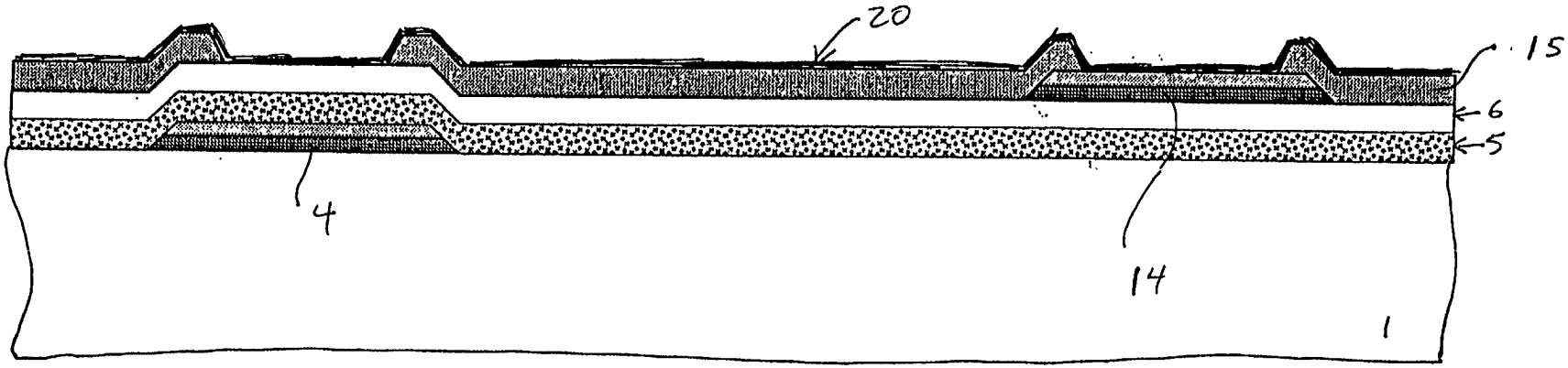


FIG. 12B

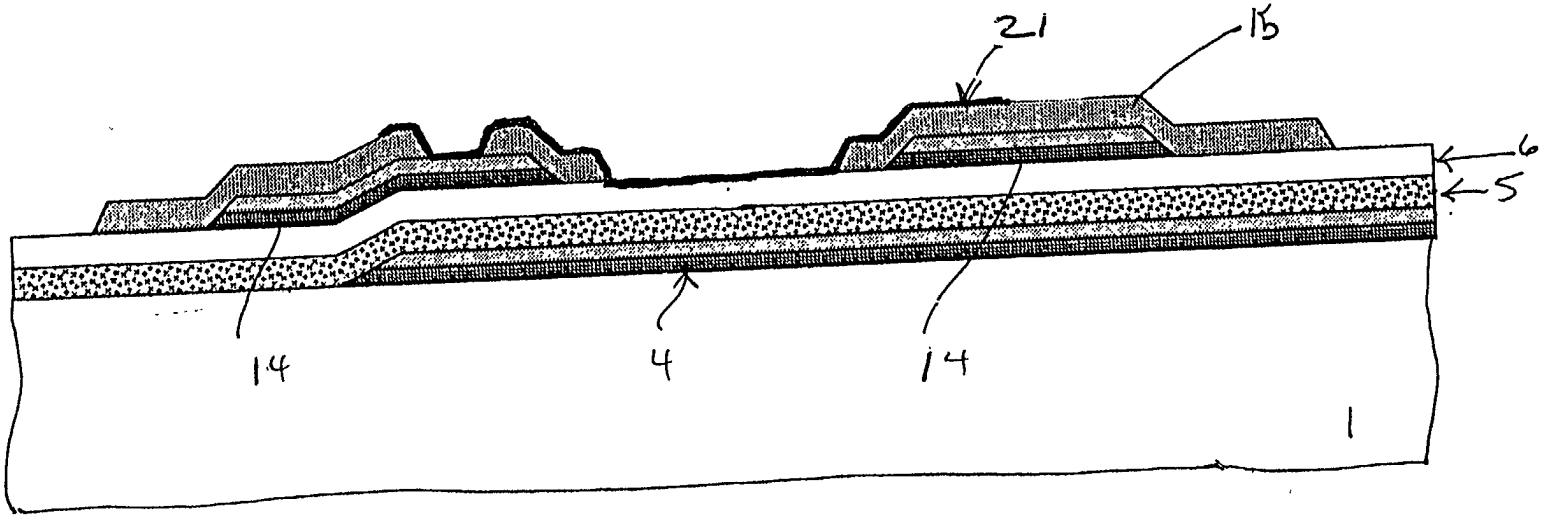


FIG. 13A

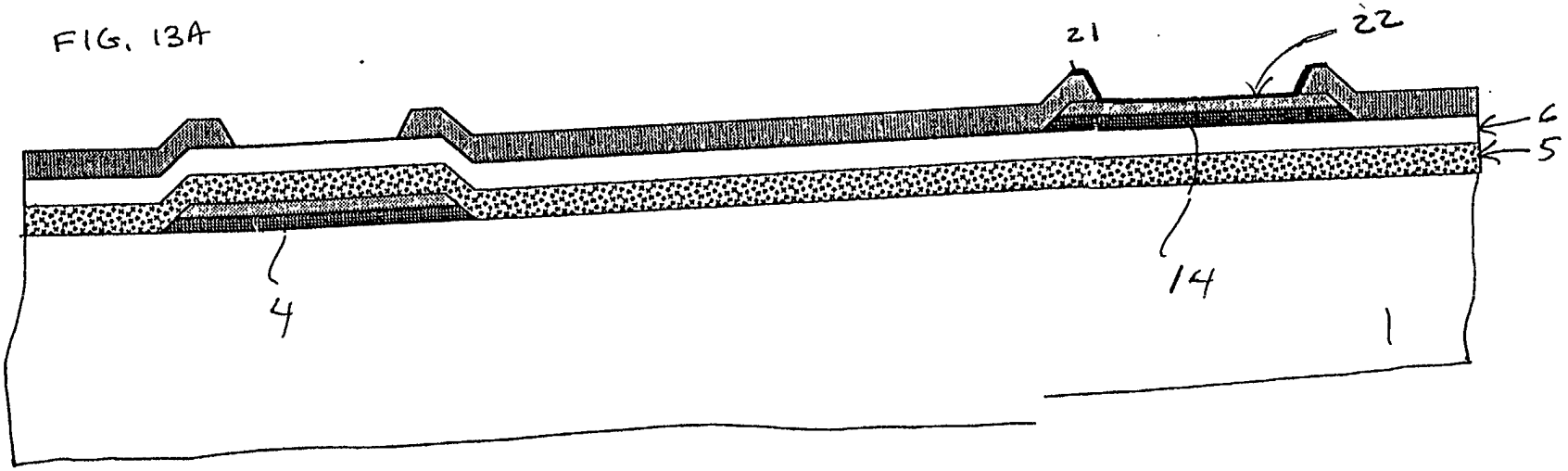


FIG. 13B

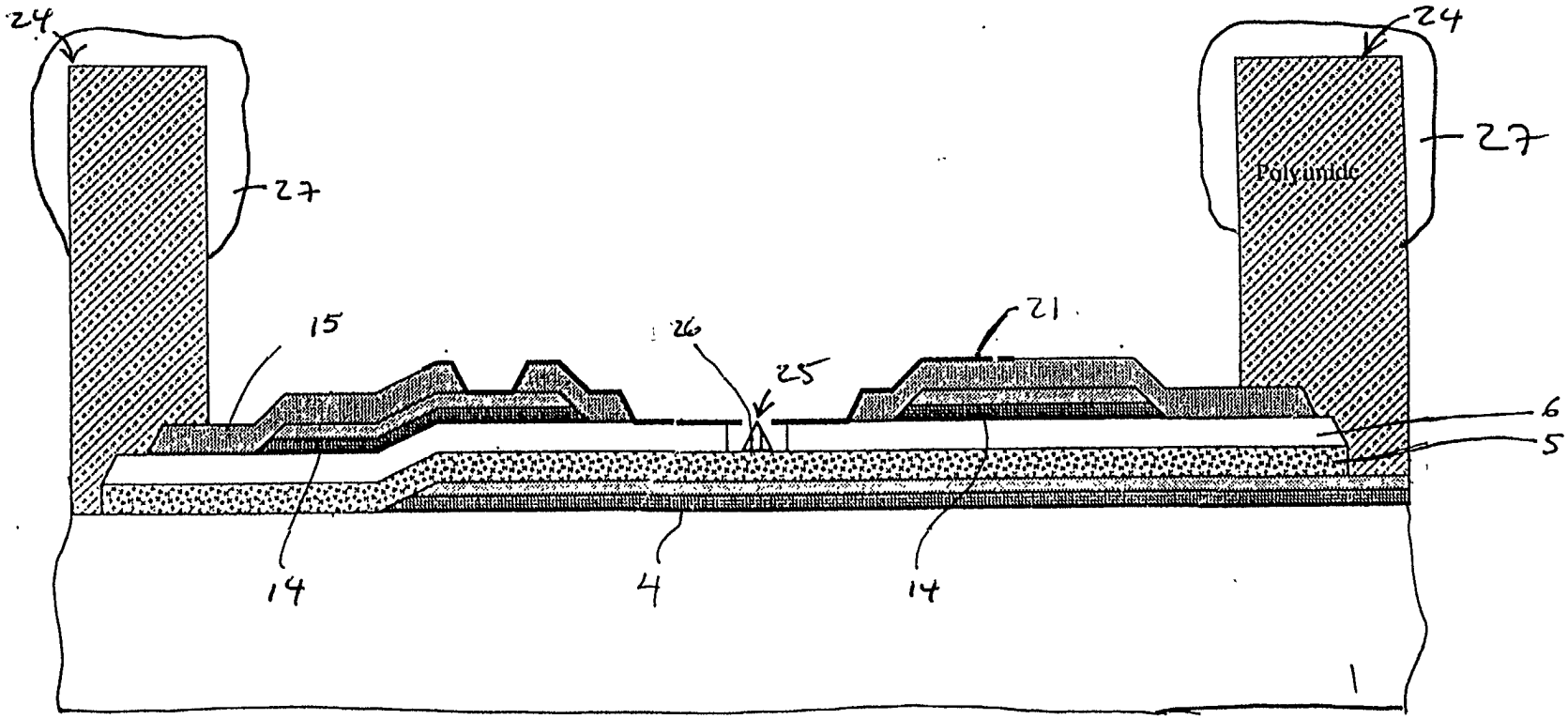


FIG. 14A

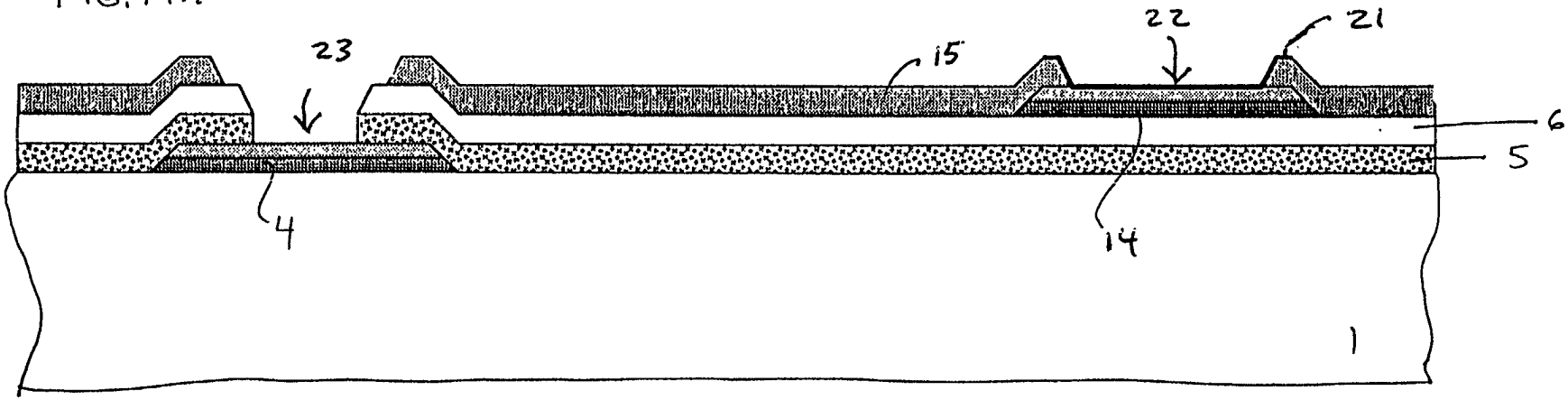
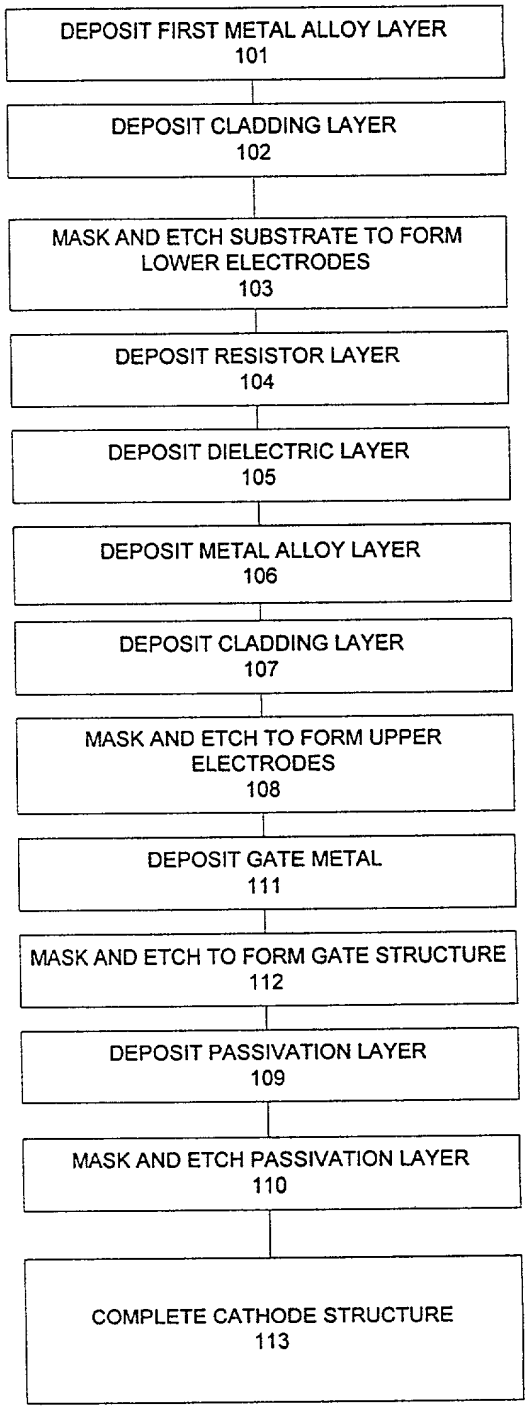


FIG. 14B


DEPOSIT FIRST METAL ALLOY LAYER
101
DEPOSIT CLADDING LAYER
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MASK AND ETCH SUBSTRATE TO FORM LOWER ELECTRODES
103
DEPOSIT RESISTOR LAYER
104
DEPOSIT DIELECTRIC LAYER
105
DEPOSIT METAL ALLOY LAYER
106
DEPOSIT CLADDING LAYER
107
MASK AND ETCH TO FORM UPPER ELECTRODES
108
DEPOSIT GATE METAL
111
MASK AND ETCH TO FORM GATE STRUCTURE
112
DEPOSIT PASSIVATION LAYER
109
MASK AND ETCH PASSIVATION LAYER
110
COMPLETE CATHODE STRUCTURE
113

FIG. 15

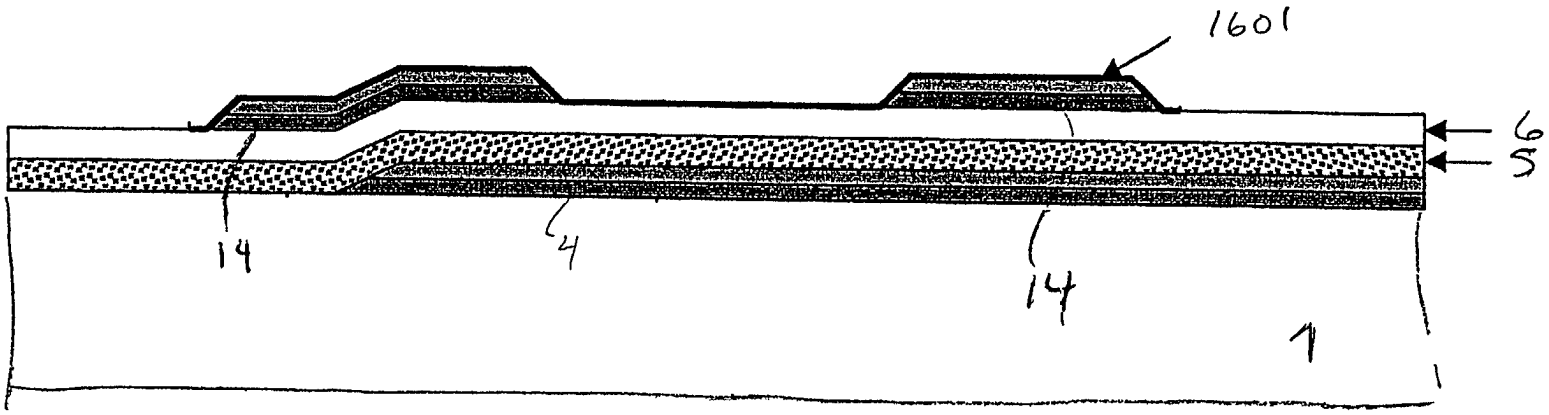


FIG. 16A

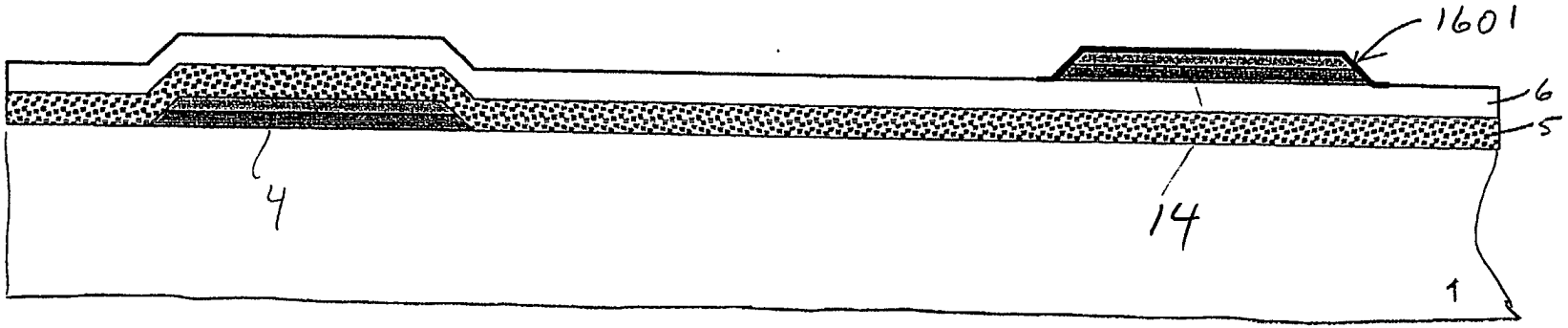


FIG. 16B

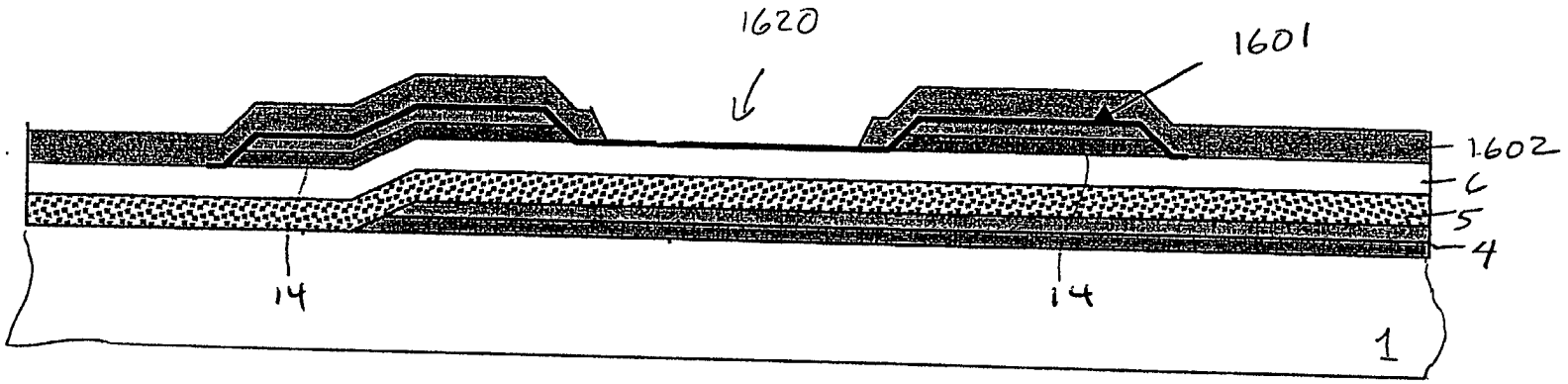


FIG. 16C

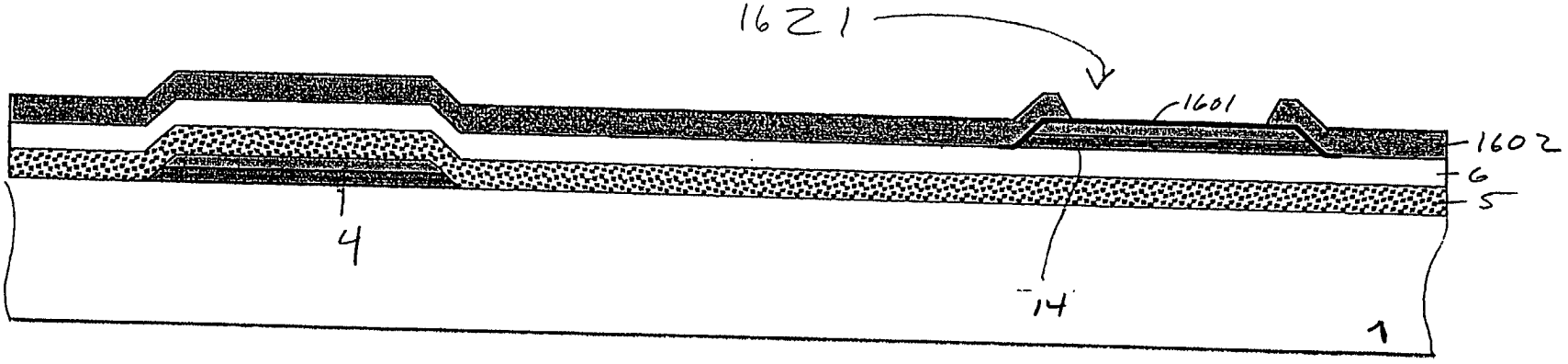


FIG. 16D

FIG. 16E

FIG. 16F

FIG 16G

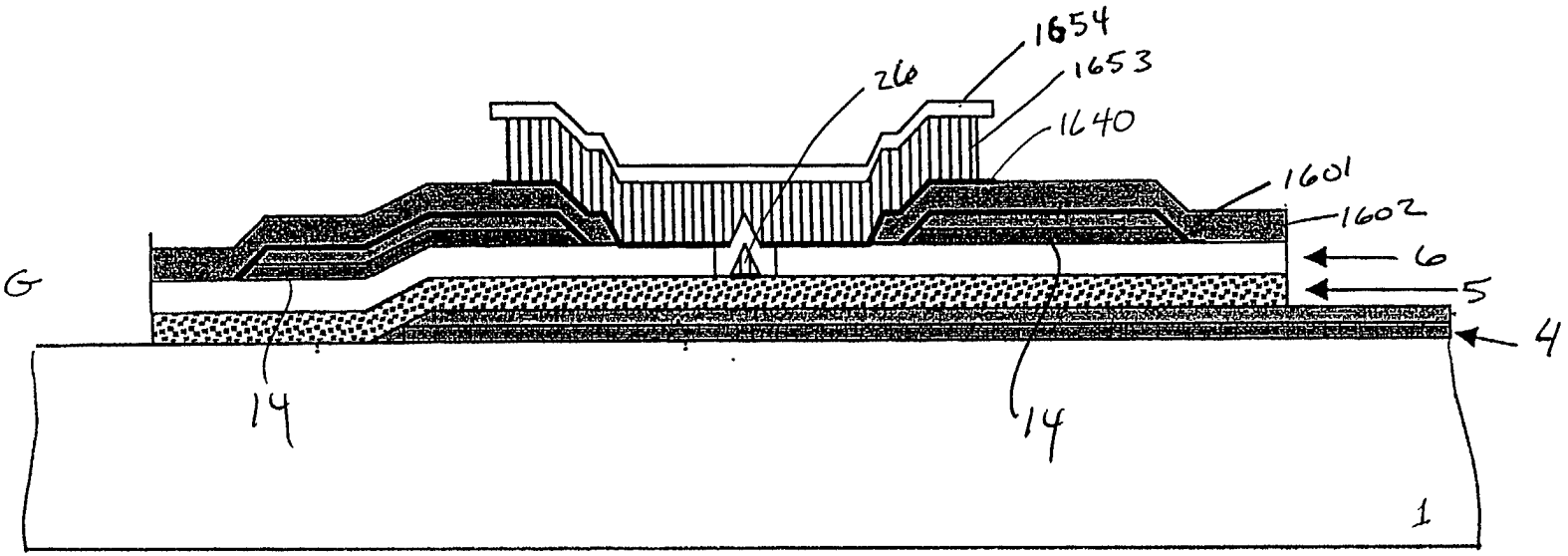
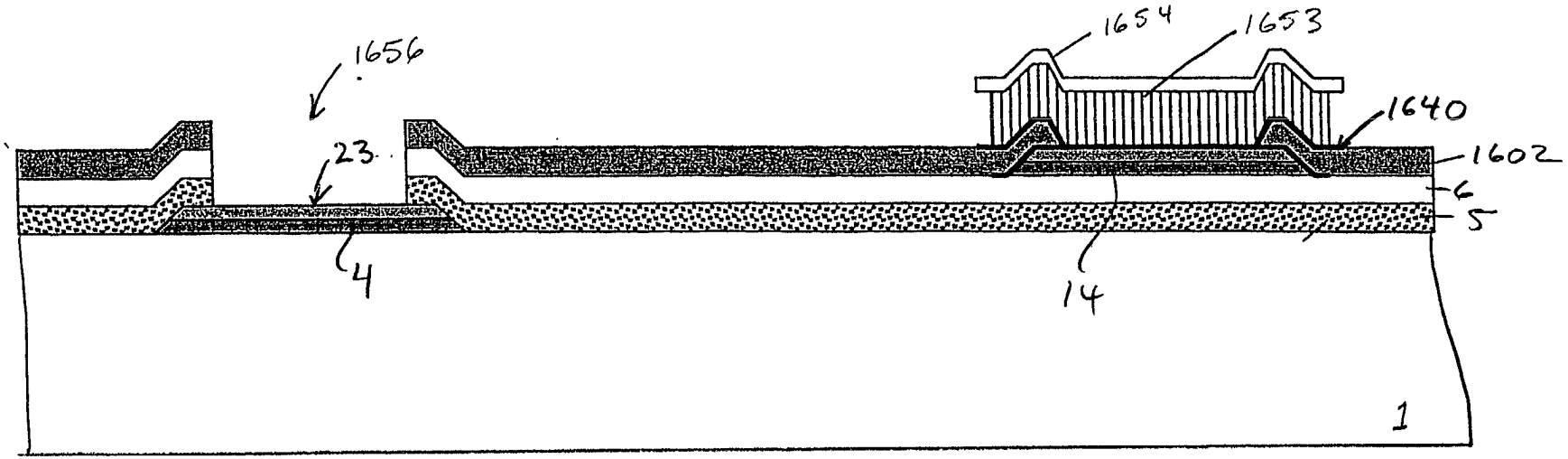


FIG 16H



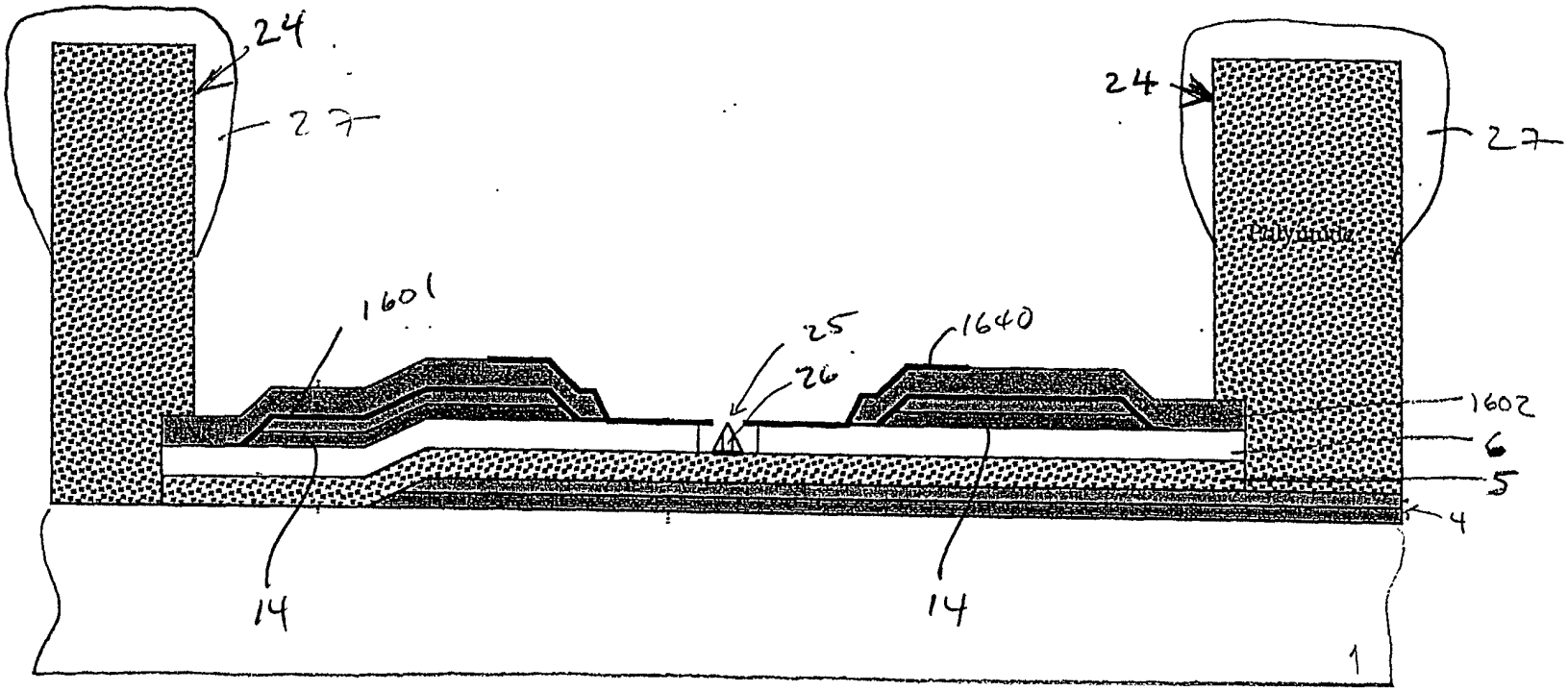


FIG 16 I

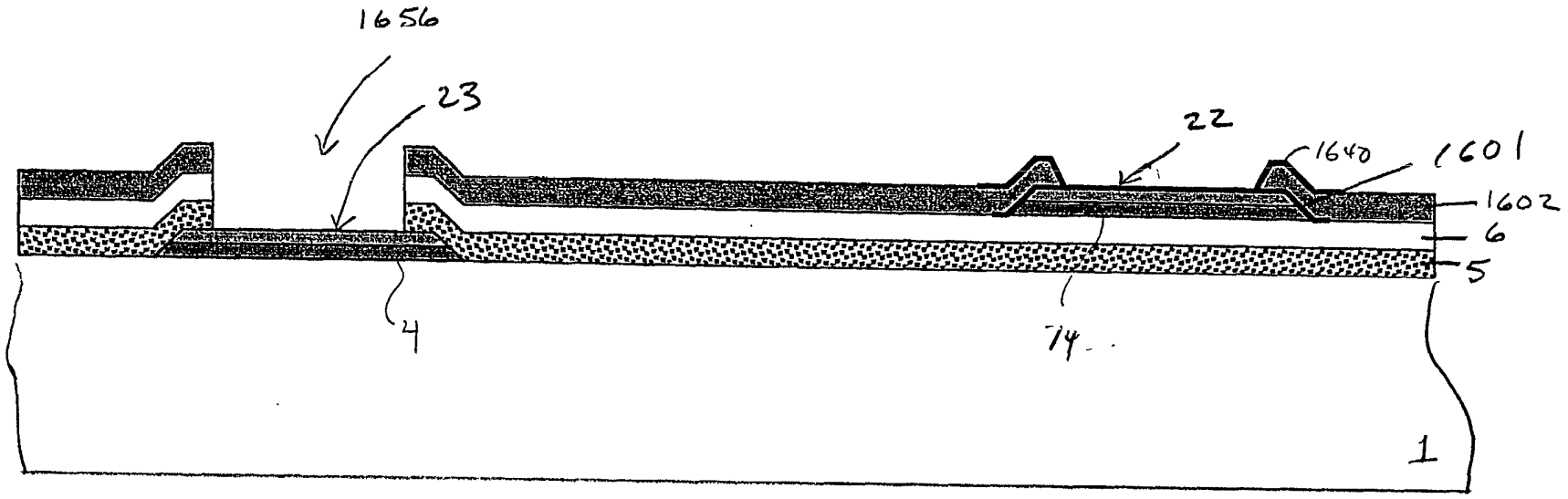


FIG 16 J

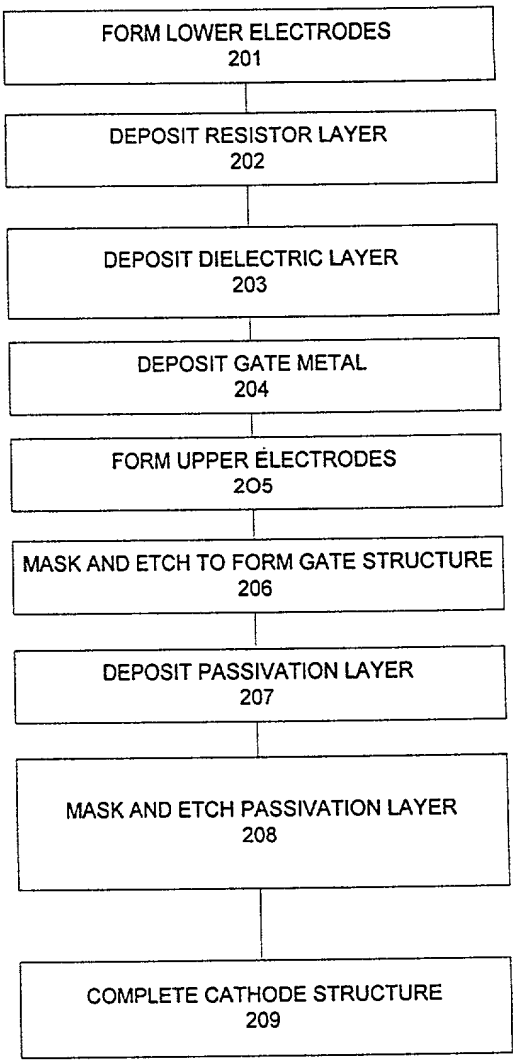

FORM LOWER ELECTRODES
201
DEPOSIT RESISTOR LAYER
202
DEPOSIT DIELECTRIC LAYER
203
DEPOSIT GATE METAL
204
FORM UPPER ELECTRODES
205
MASK AND ETCH TO FORM GATE STRUCTURE
206
DEPOSIT PASSIVATION LAYER
207
MASK AND ETCH PASSIVATION LAYER
208
COMPLETE CATHODE STRUCTURE
209

FIG. 17

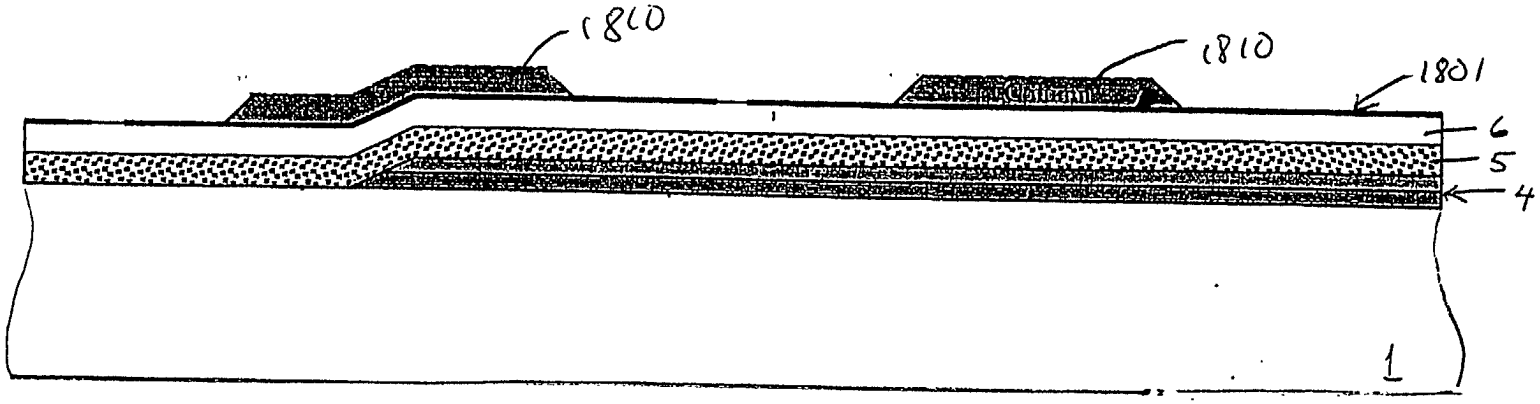


FIG 18A

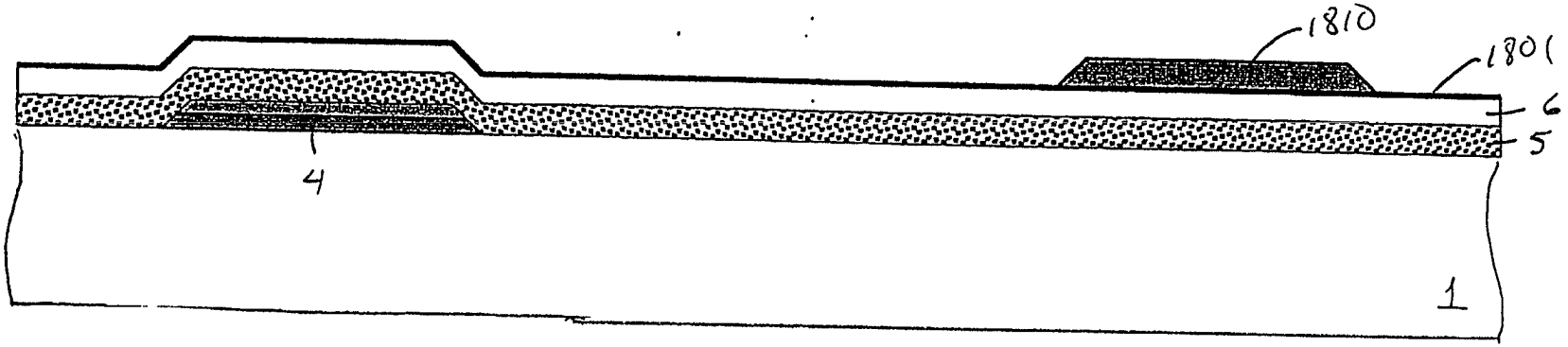


FIG 18B

FIG. 18C

FIG. 18D

FIG. 18E

FIG. 18F

FIG 18G

FIG. 18H

FIG 18 I

FIG 18 J

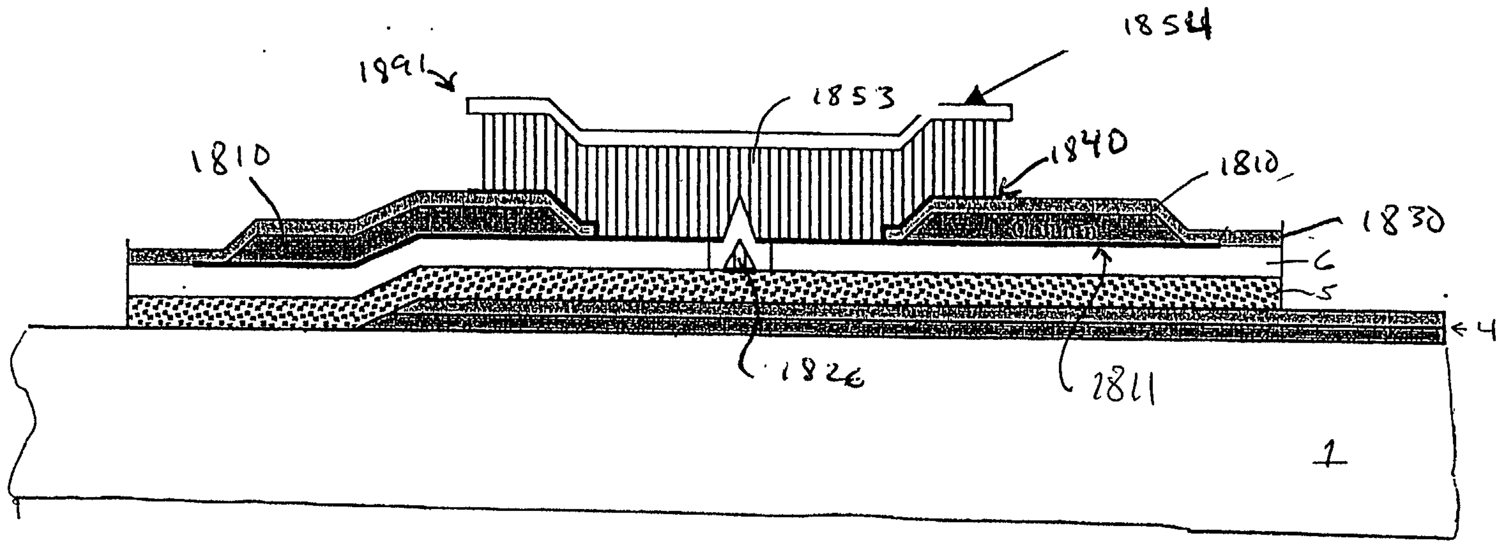


FIG 18 K

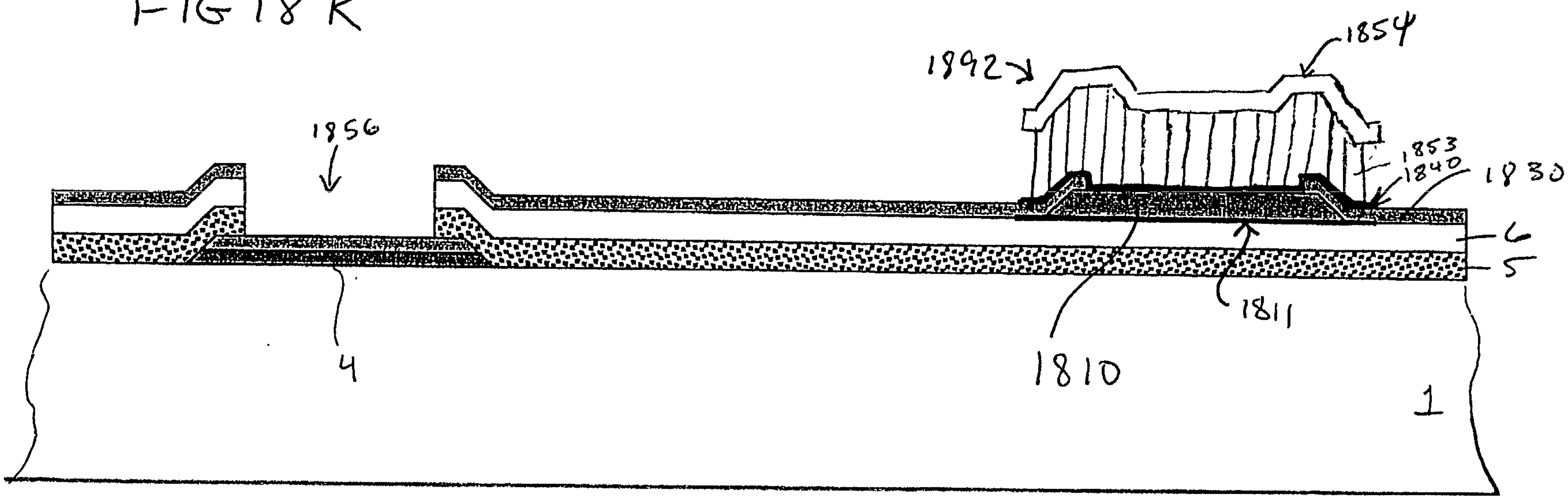


FIG 18L

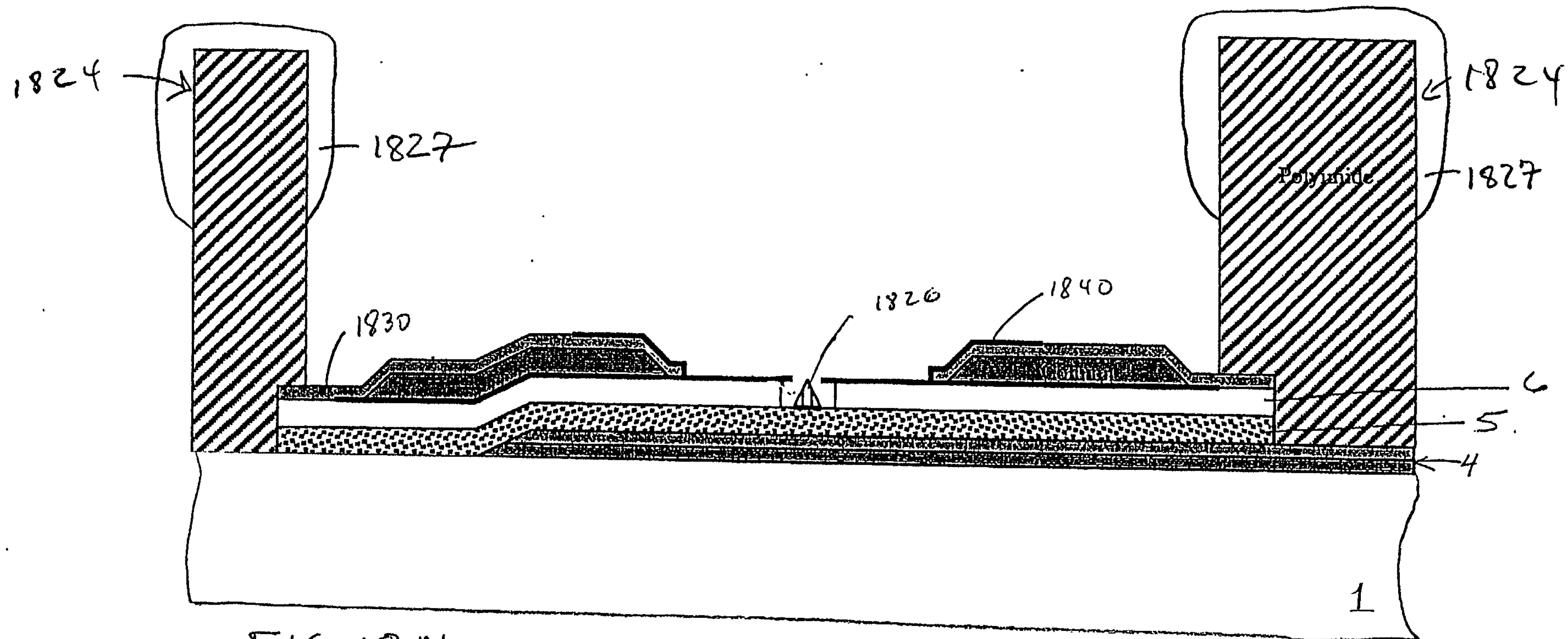


FIG 18M

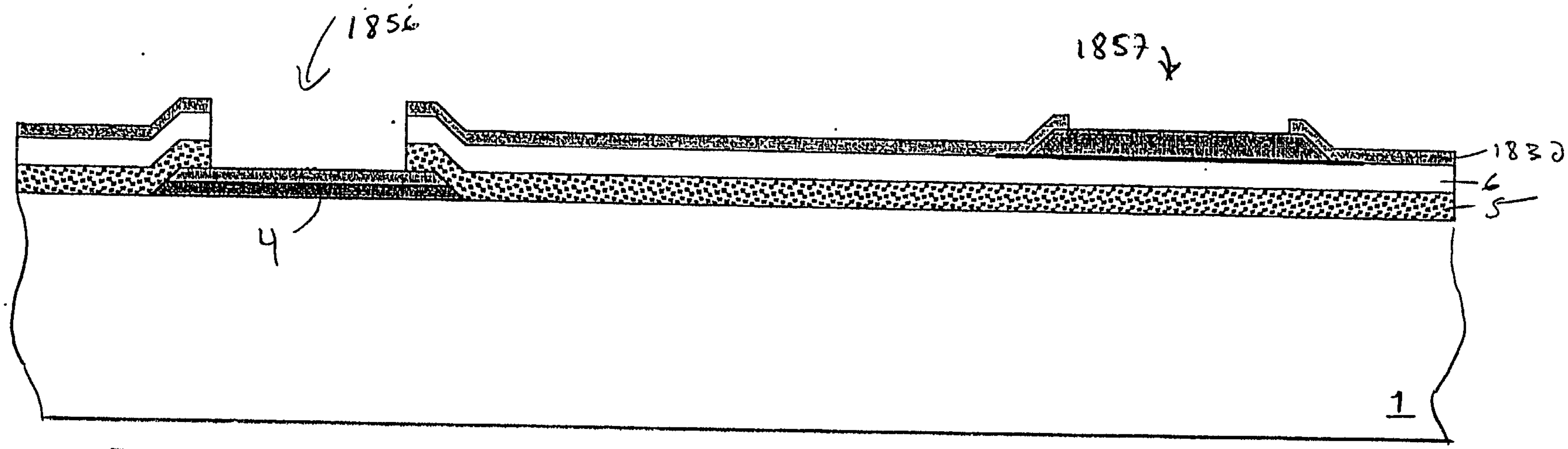


FIG 18N

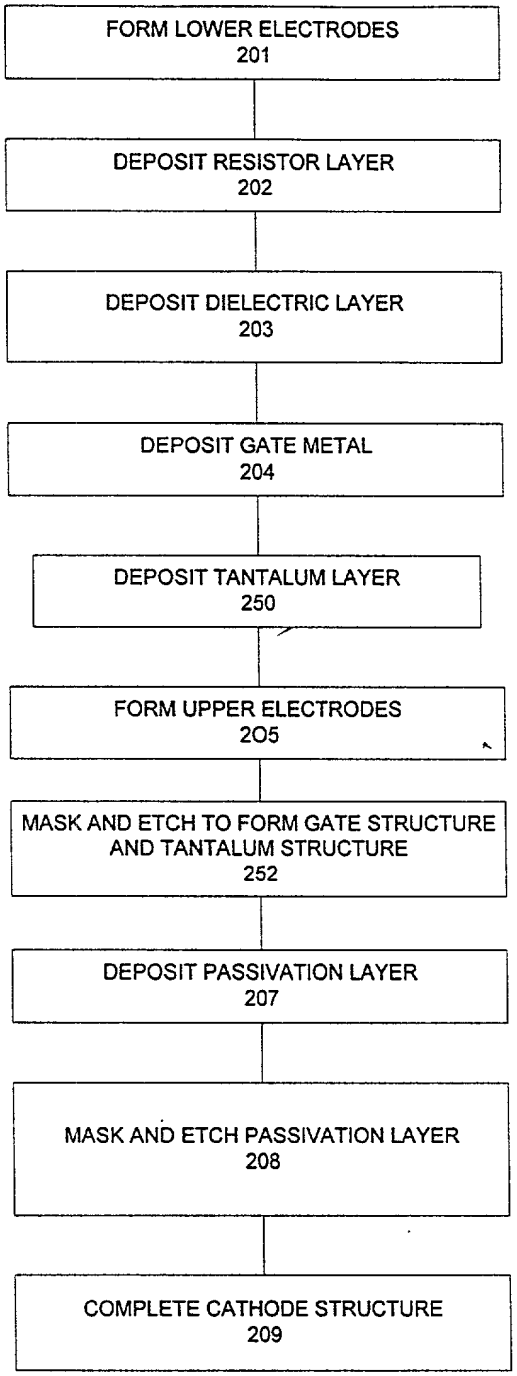

FORM LOWER ELECTRODES
201
DEPOSIT RESISTOR LAYER
202
DEPOSIT DIELECTRIC LAYER
203
DEPOSIT GATE METAL
204
DEPOSIT TANTALUM LAYER
250
FORM UPPER ELECTRODES
205
MASK AND ETCH TO FORM GATE STRUCTURE AND TANTALUM STRUCTURE
252
DEPOSIT PASSIVATION LAYER
207
MASK AND ETCH PASSIVATION LAYER
208
COMPLETE CATHODE STRUCTURE
209

FIG. 19

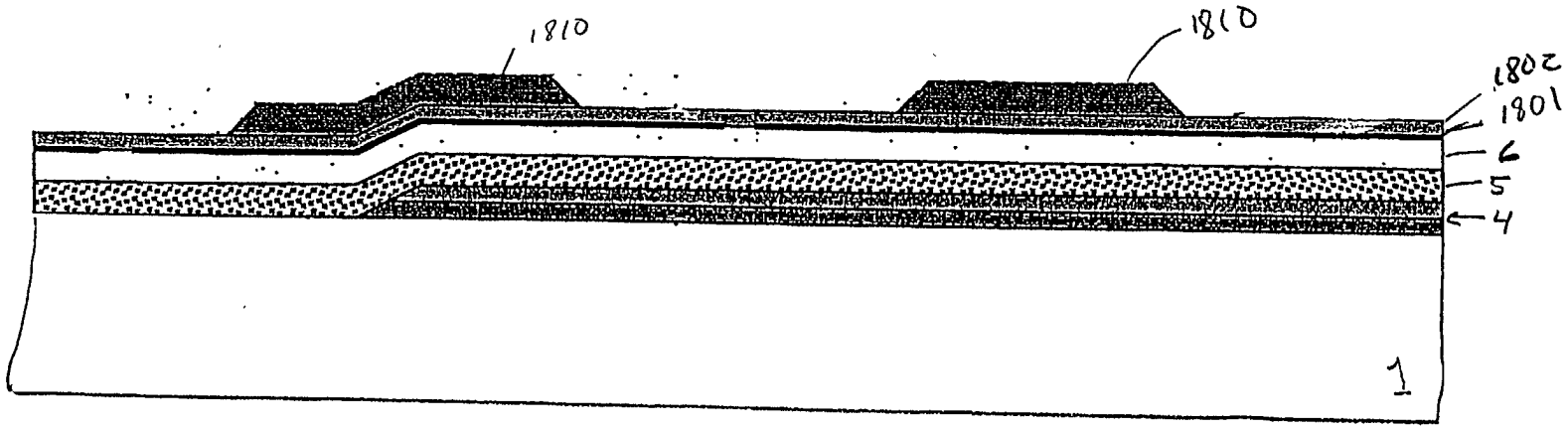


FIG. 20A

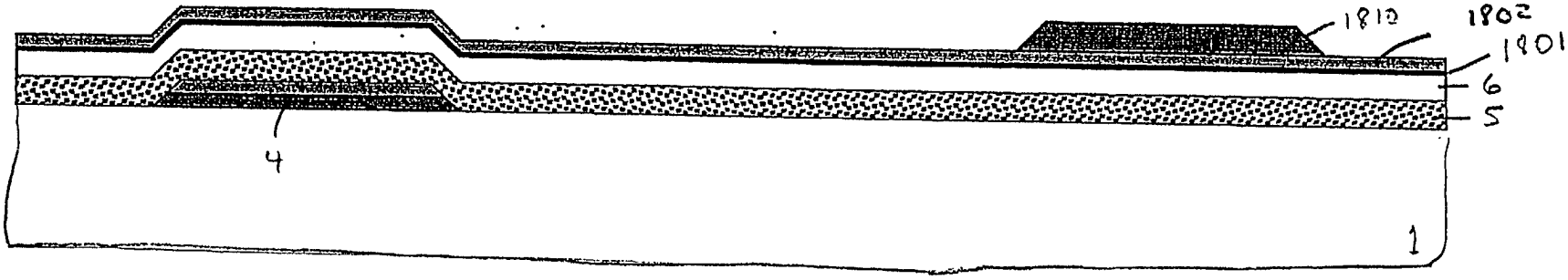


FIG. 20B

FIG. 20C

FIG. 20D

FIG 20F

FIG 20E

FIG. 20H

FIG. 20G

FIG. 20J

FIG. 20I

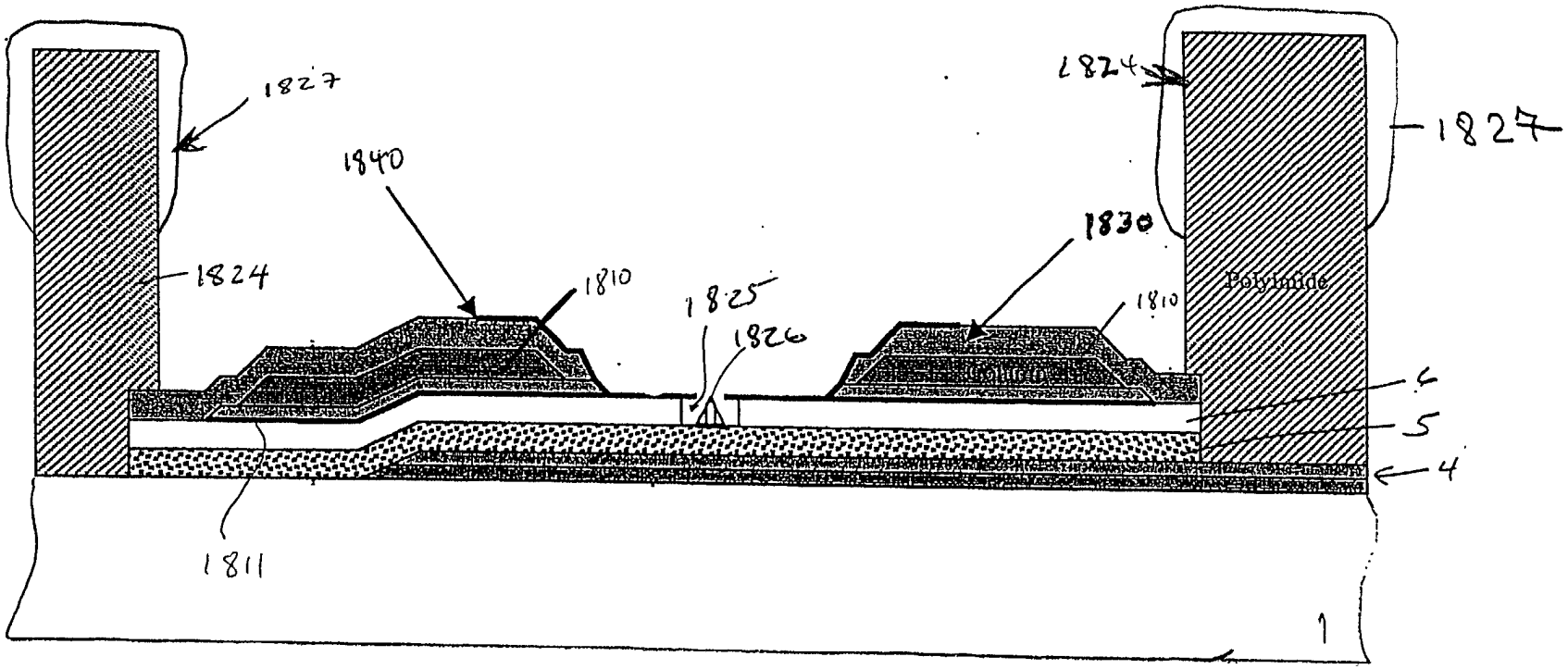


FIG 20K

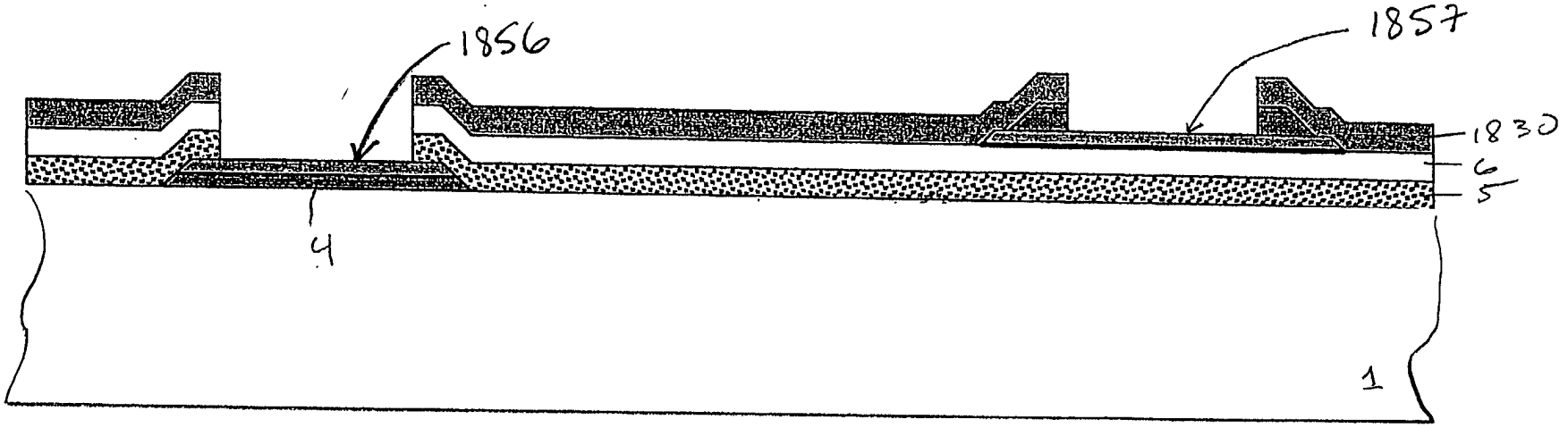


FIG 20L

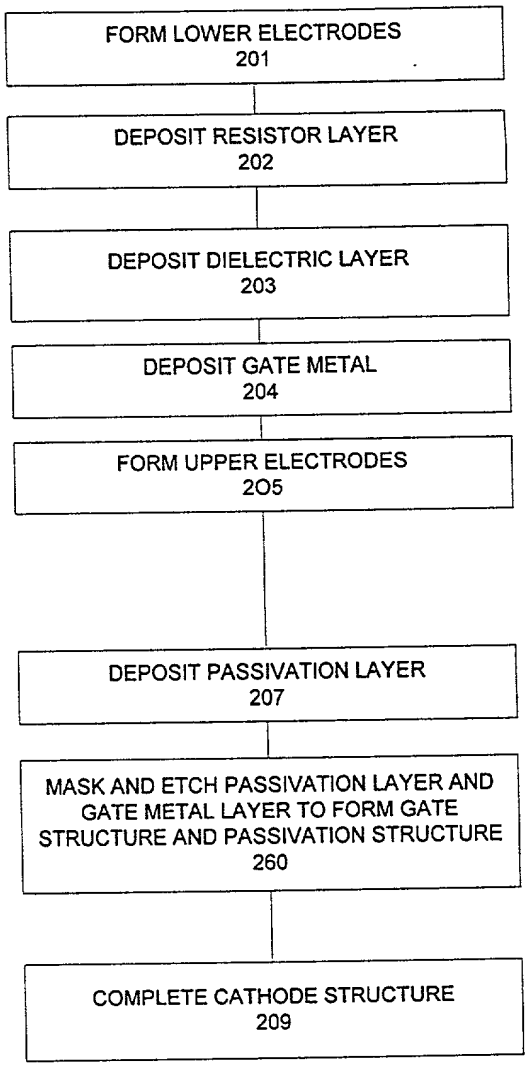

FORM LOWER ELECTRODES
201
DEPOSIT RESISTOR LAYER
202
DEPOSIT DIELECTRIC LAYER
203
DEPOSIT GATE METAL
204
FORM UPPER ELECTRODES
2O5
DEPOSIT PASSIVATION LAYER
207
MASK AND ETCH PASSIVATION LAYER AND GATE METAL LAYER TO FORM GATE STRUCTURE AND PASSIVATION STRUCTURE
260
COMPLETE CATHODE STRUCTURE
209

FIG. 21

FIG. 22A

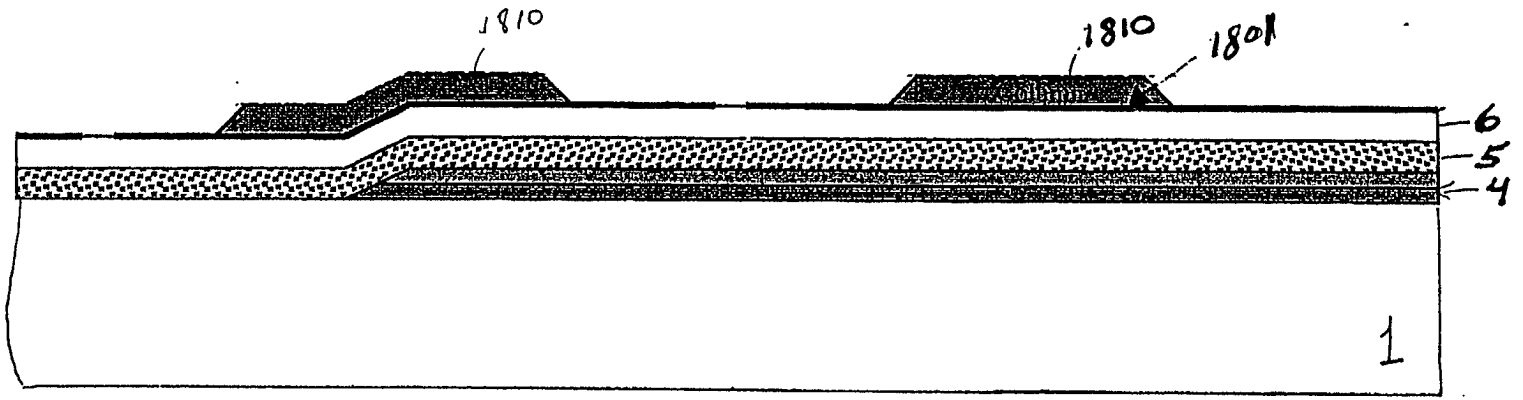


FIG. 22B

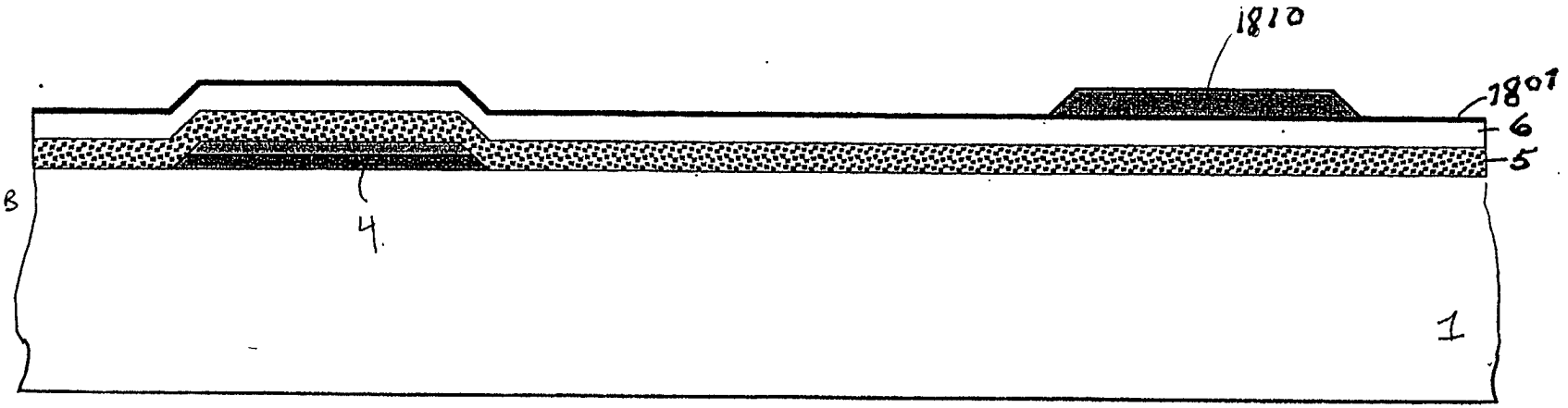


FIG. 22C

FIG. 22D

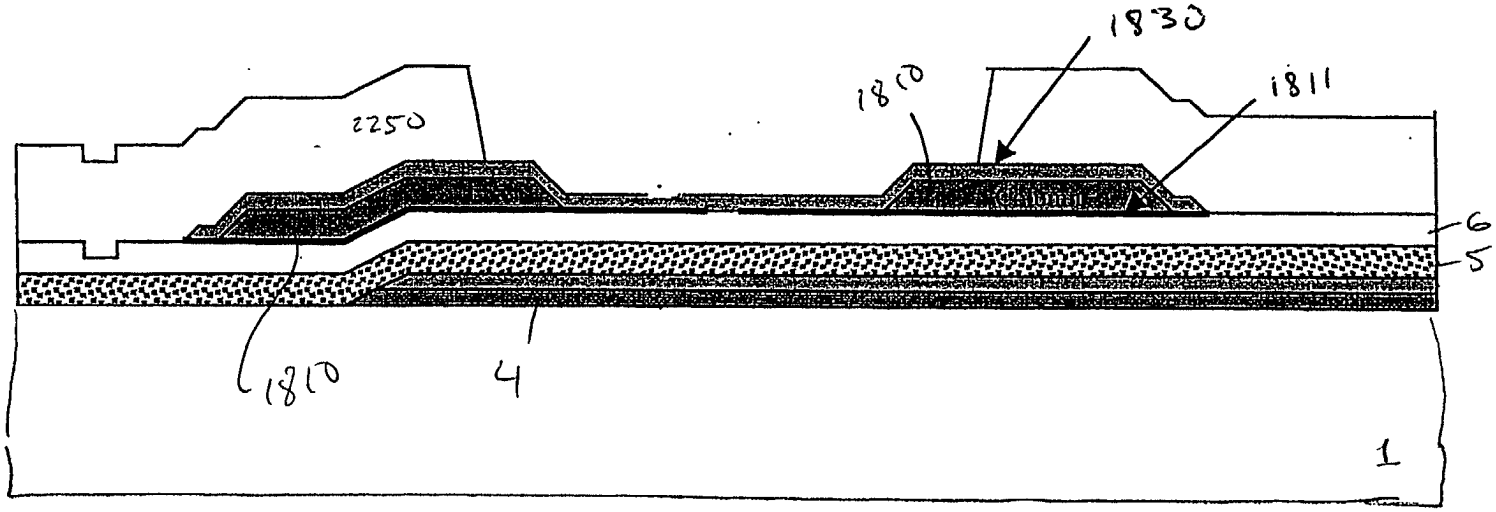


FIG 22E

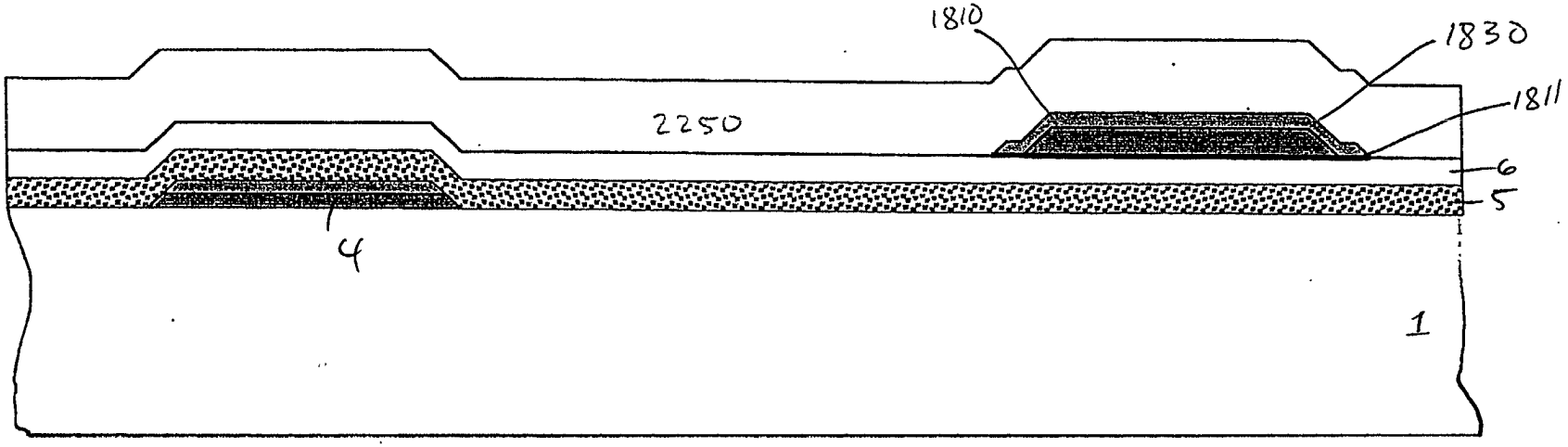


FIG22F

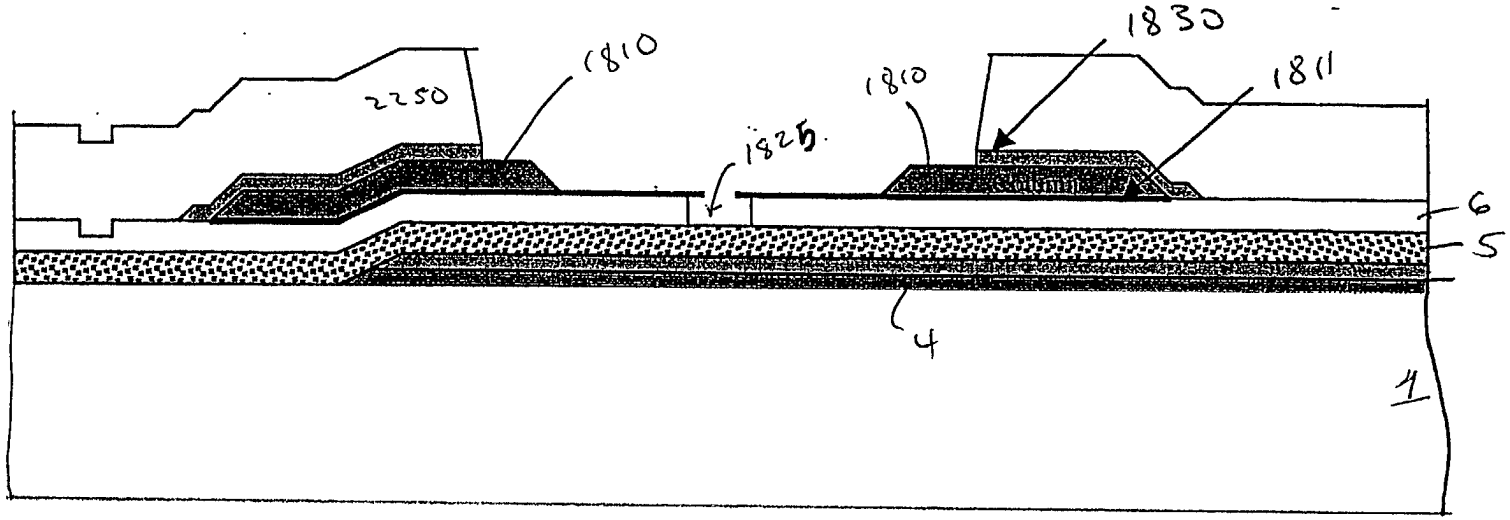


FIG 22G

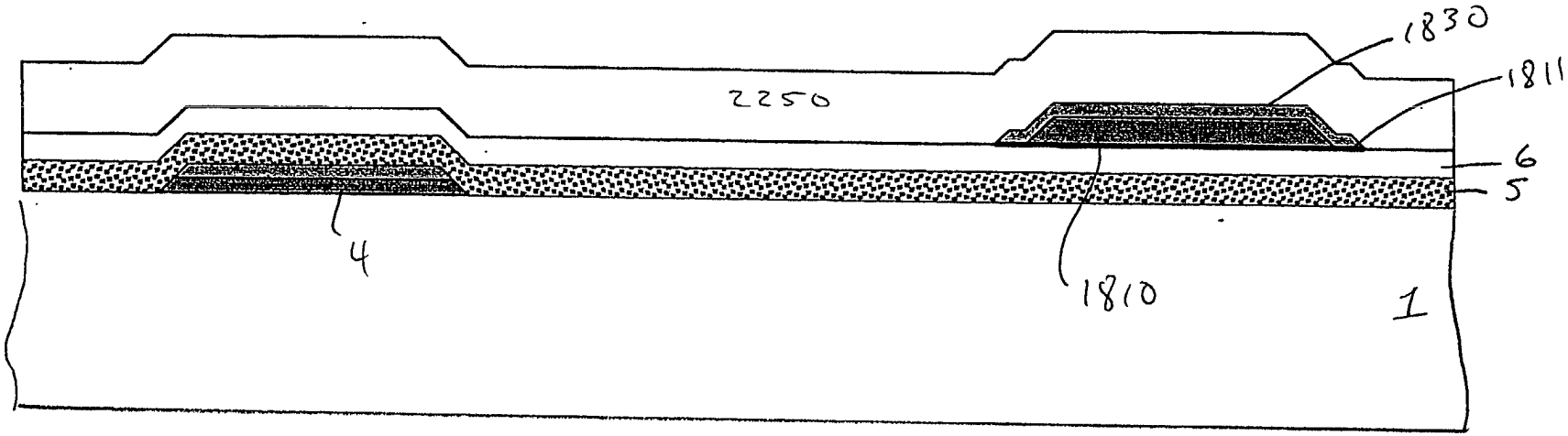


FIG 22H

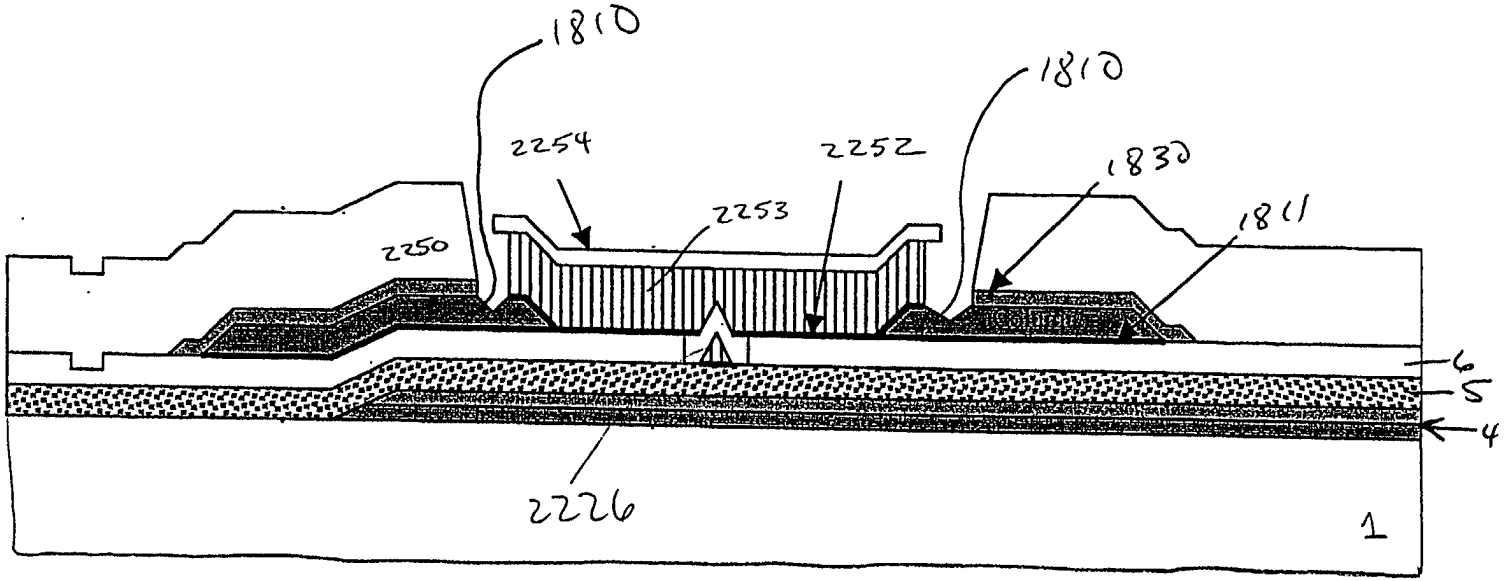


FIG.22I

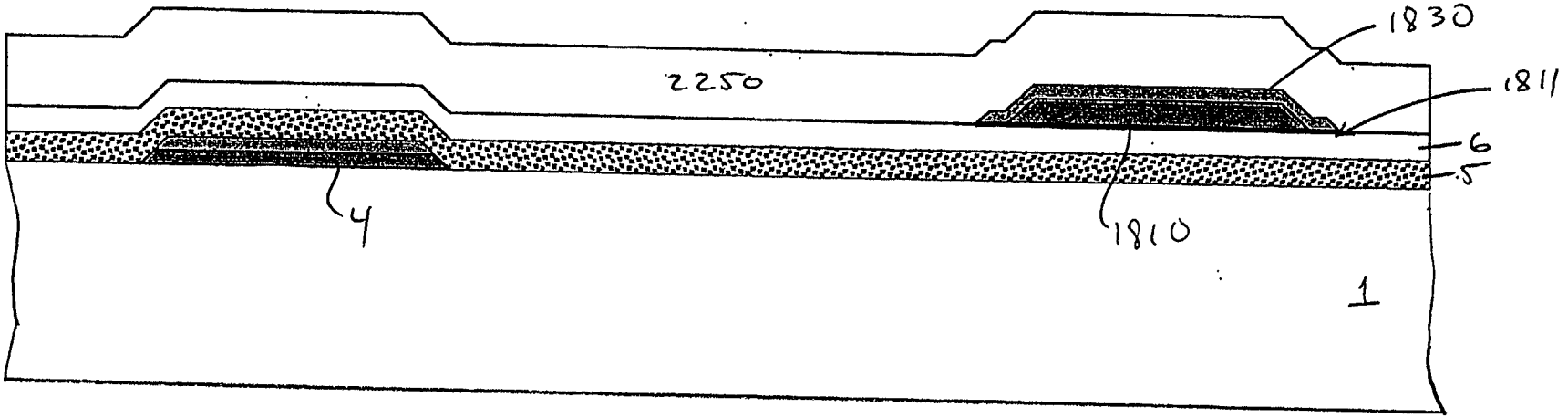


FIG.22J

FIG. 22K

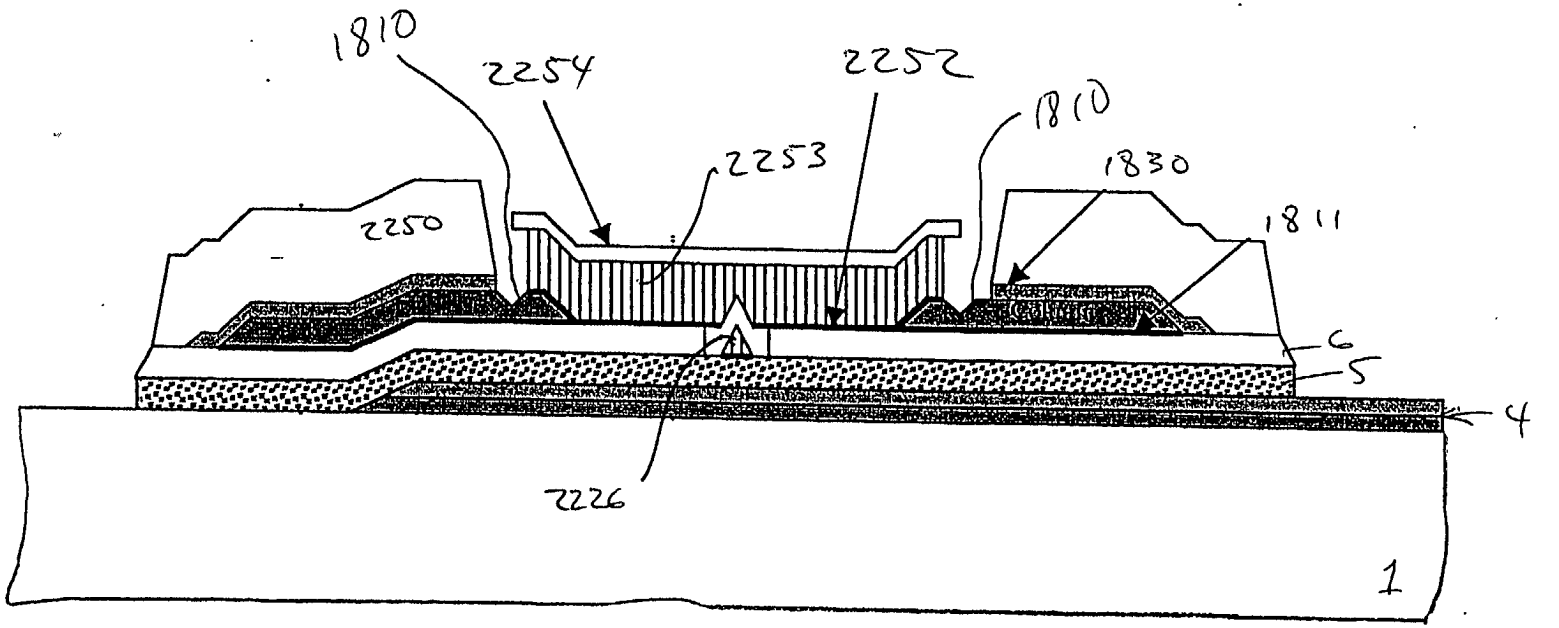
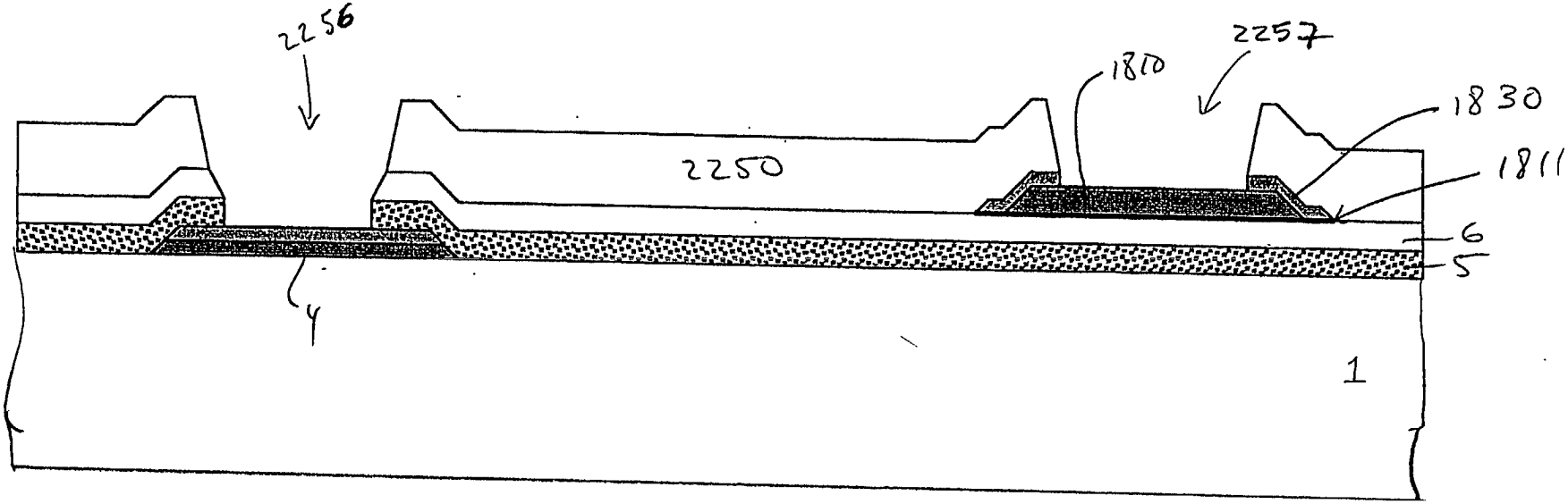


FIG 22L



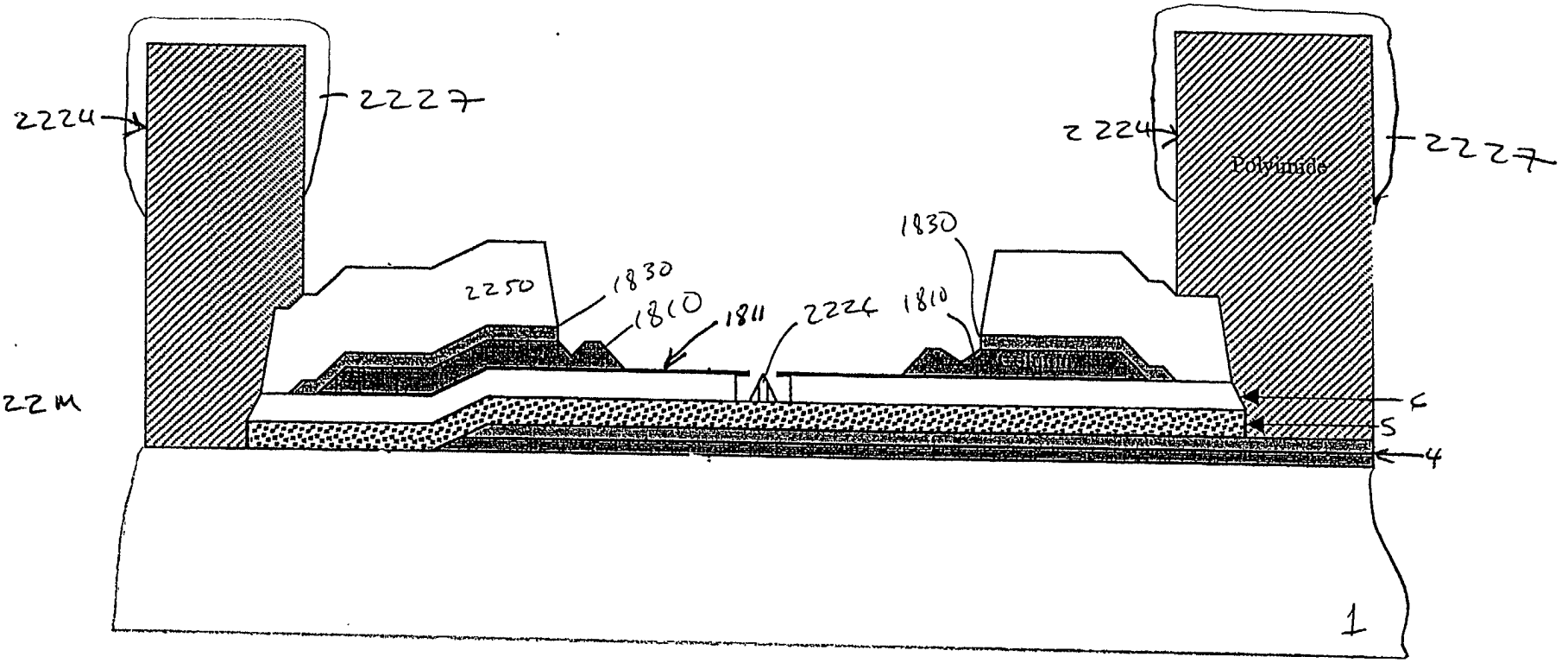


FIG 22M

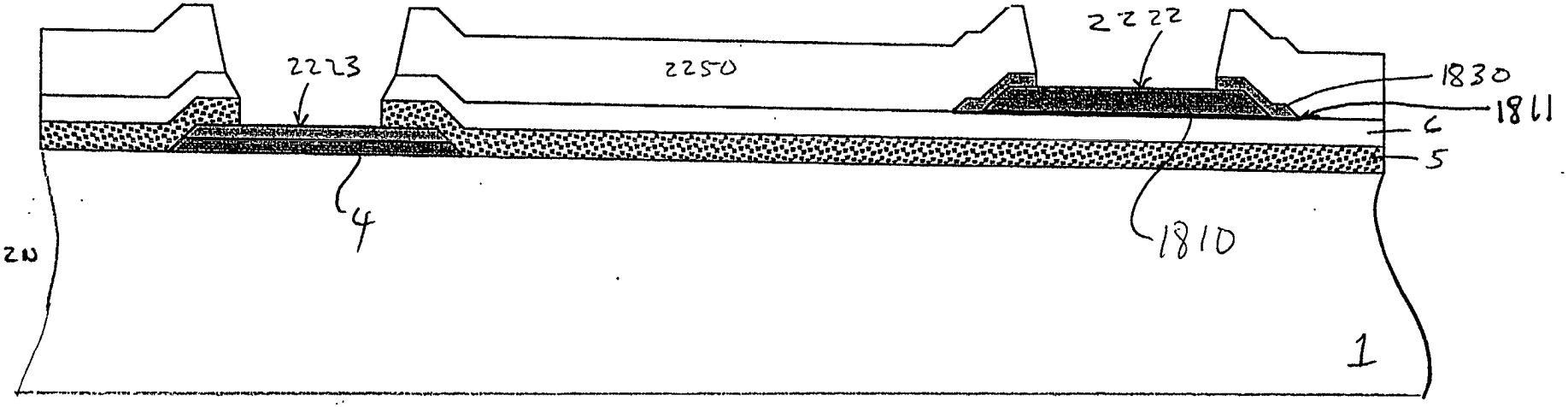


FIG 22N

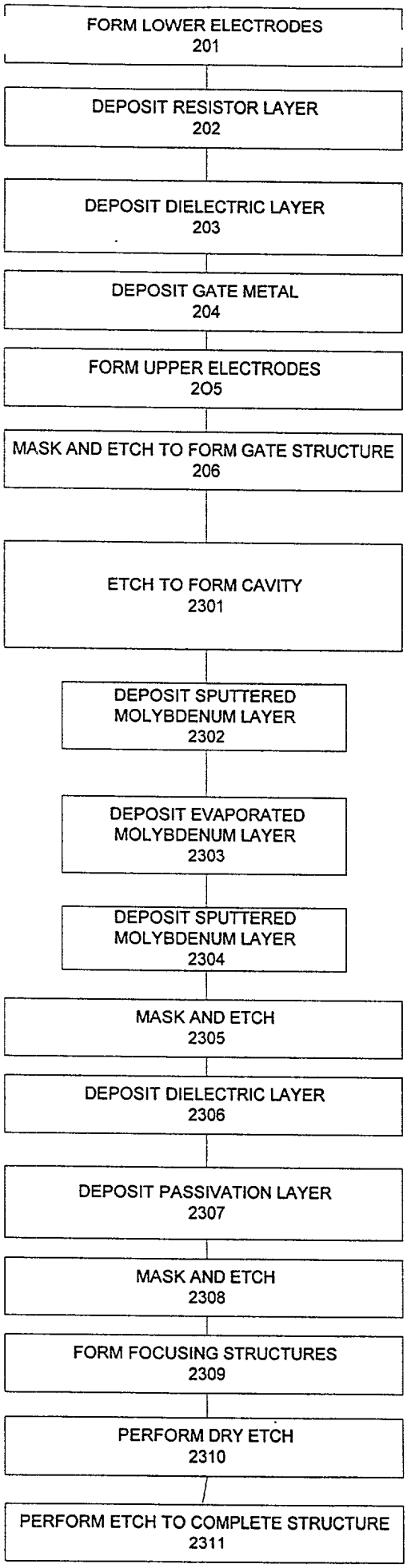

FORM LOWER ELECTRODES
201
DEPOSIT RESISTOR LAYER
202
DEPOSIT DIELECTRIC LAYER
203
DEPOSIT GATE METAL
204
FORM UPPER ELECTRODES
2O5
MASK AND ETCH TO FORM GATE STRUCTURE
206
ETCH TO FORM CAVITY
2301
DEPOSIT SPUTTERED MOLYBDENUM LAYER
2302
DEPOSIT EVAPORATED MOLYBDENUM LAYER
2303
DEPOSIT SPUTTERED MOLYBDENUM LAYER
2304
MASK AND ETCH
2305
DEPOSIT DIELECTRIC LAYER
2306
DEPOSIT PASSIVATION LAYER
2307
MASK AND ETCH
2308
FORM FOCUSING STRUCTURES
2309
PERFORM DRY ETCH
2310
PERFORM ETCH TO COMPLETE STRUCTURE
2311

FIG. 23

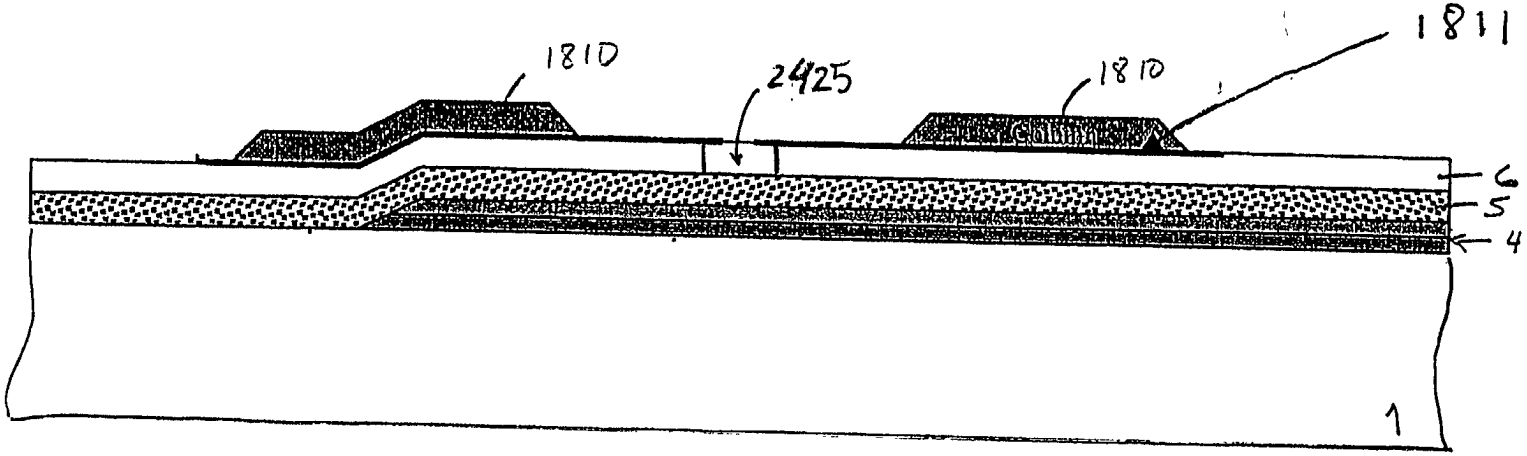


FIG 24A

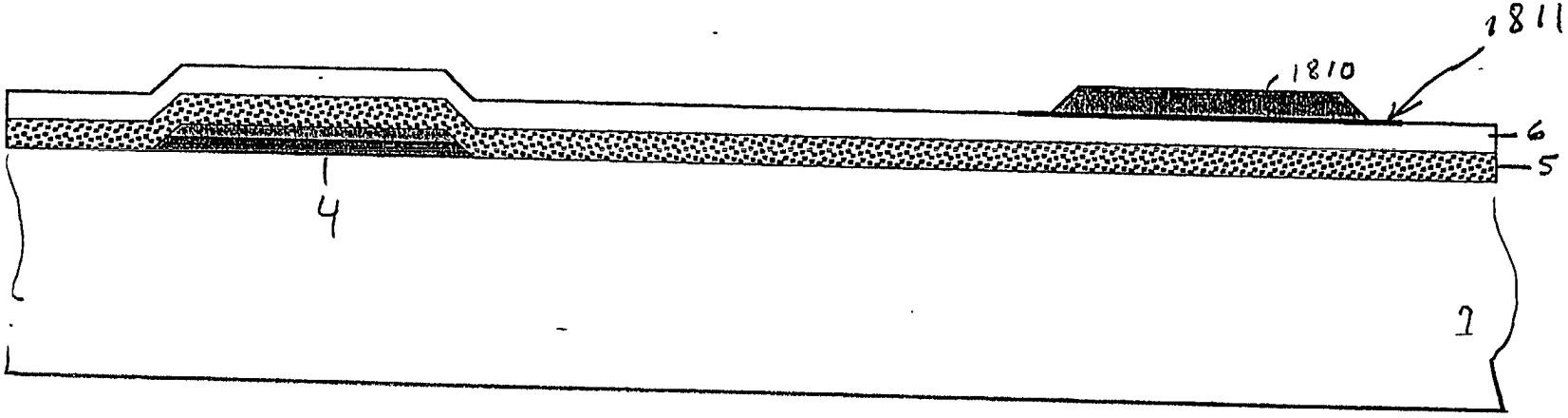


FIG. 24B

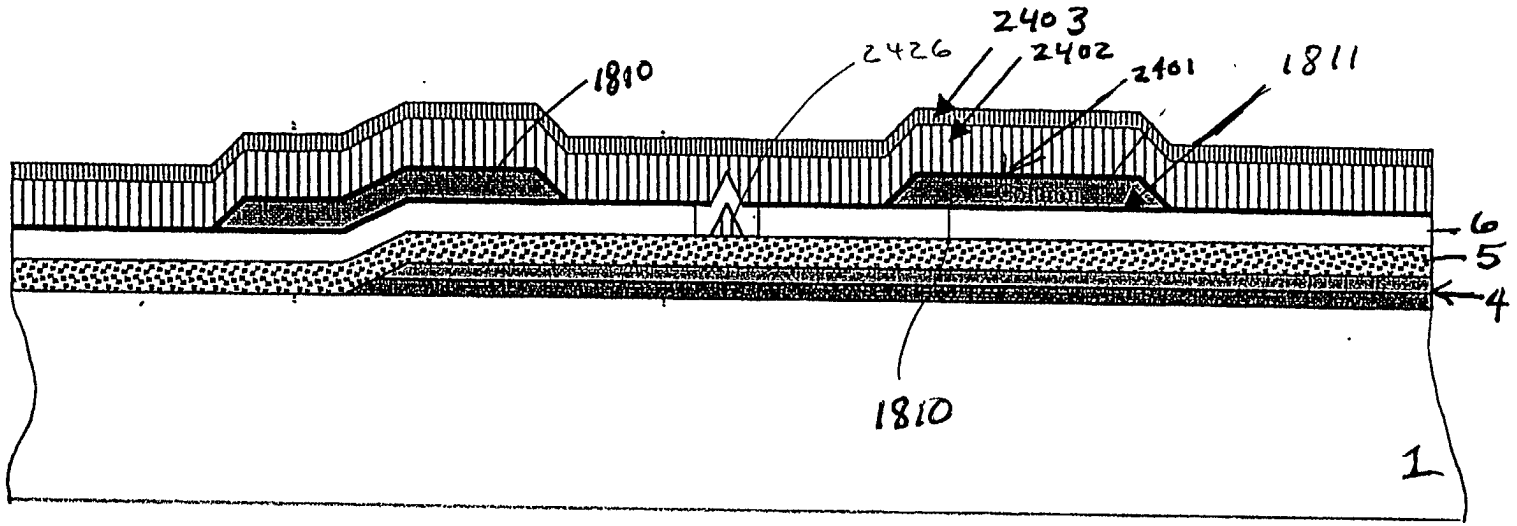


FIG 24C

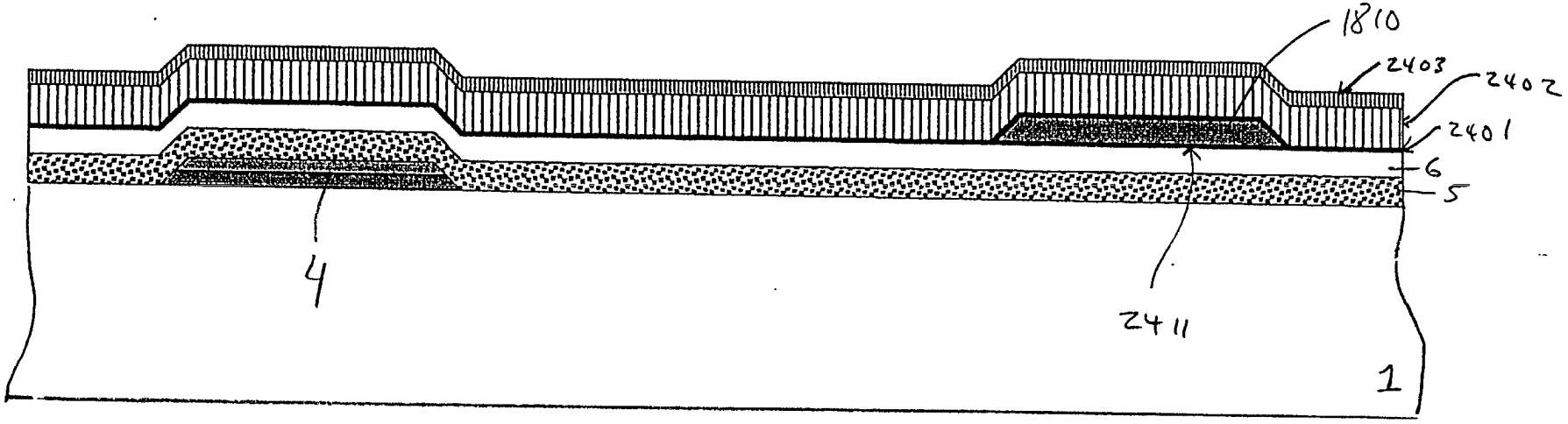


FIG 24D

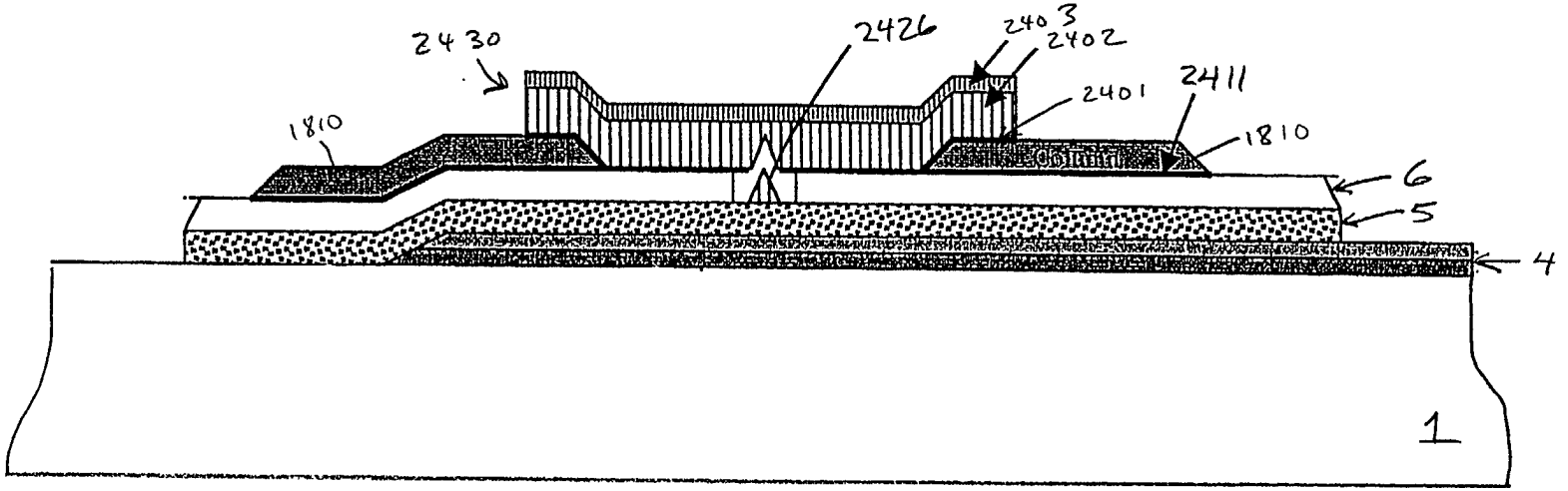


FIG 24E

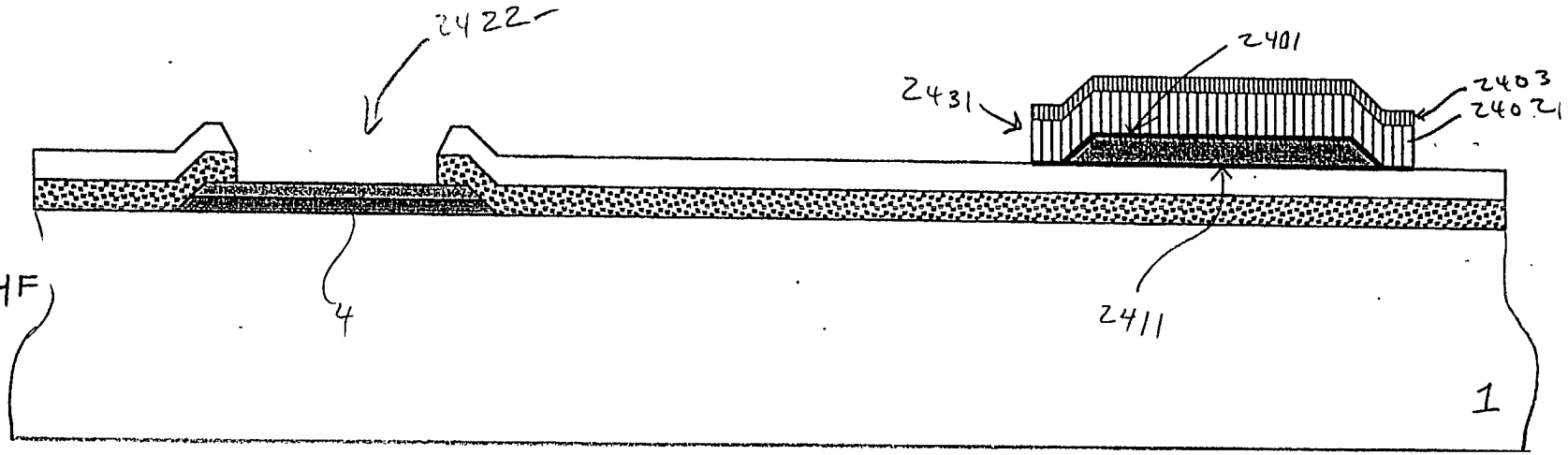


FIG 24F

Fig. 24G

Fig. 24H

FIG 24J

FIG 24I

Fig 24K

Fig 24L

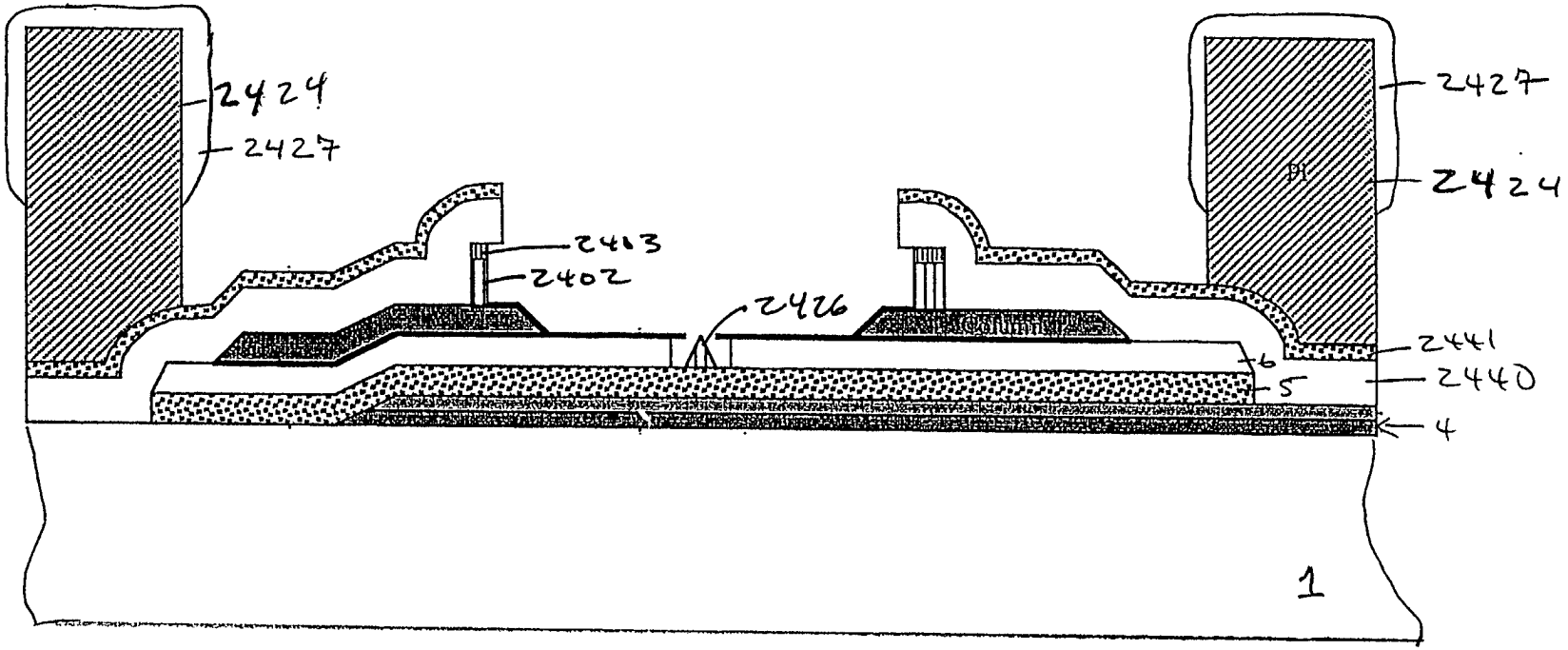


FIG. 24M

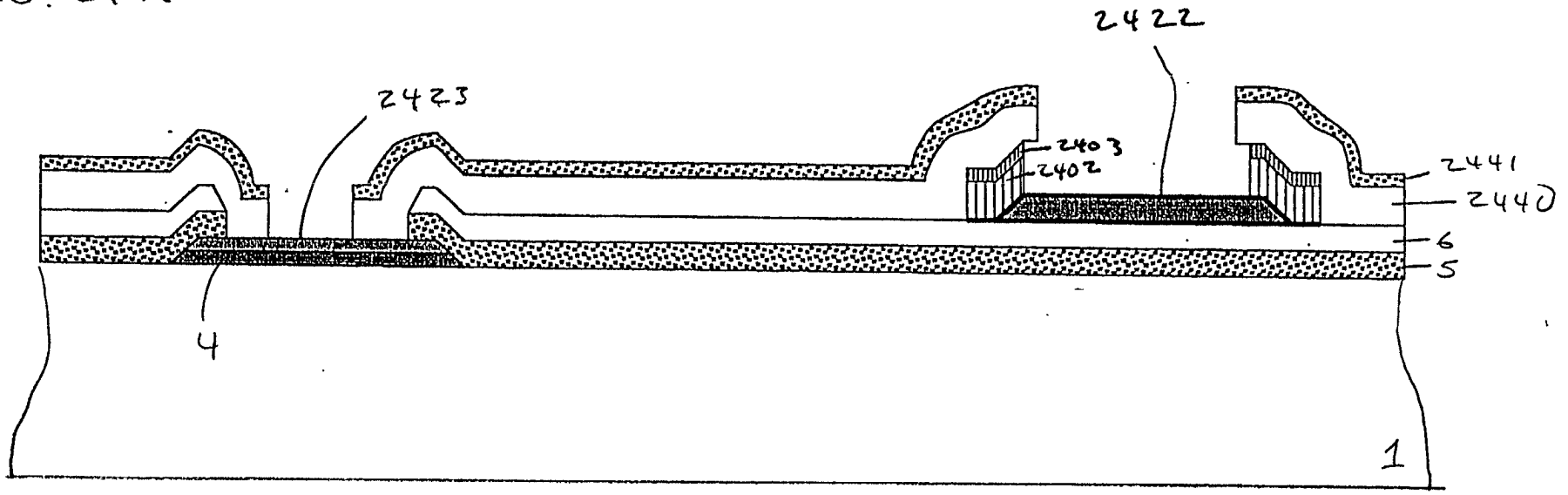


FIG. 24N

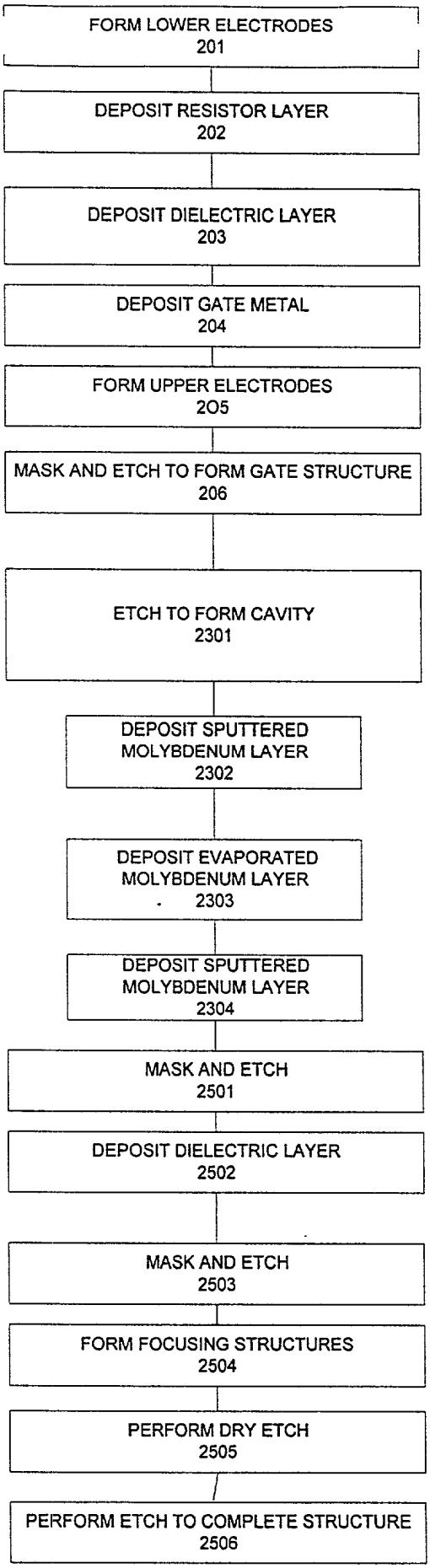

FORM LOWER ELECTRODES
201
DEPOSIT RESISTOR LAYER
202
DEPOSIT DIELECTRIC LAYER
203
DEPOSIT GATE METAL
204
FORM UPPER ELECTRODES
2O5
MASK AND ETCH TO FORM GATE STRUCTURE
206
ETCH TO FORM CAVITY
2301
DEPOSIT SPUTTERED MOLYBDENUM LAYER
2302
DEPOSIT EVAPORATED MOLYBDENUM LAYER
2303
DEPOSIT SPUTTERED MOLYBDENUM LAYER
2304
MASK AND ETCH
2501
DEPOSIT DIELECTRIC LAYER
2502
MASK AND ETCH
2503
FORM FOCUSING STRUCTURES
2504
PERFORM DRY ETCH
2505
PERFORM ETCH TO COMPLETE STRUCTURE
2506

FIG. 25

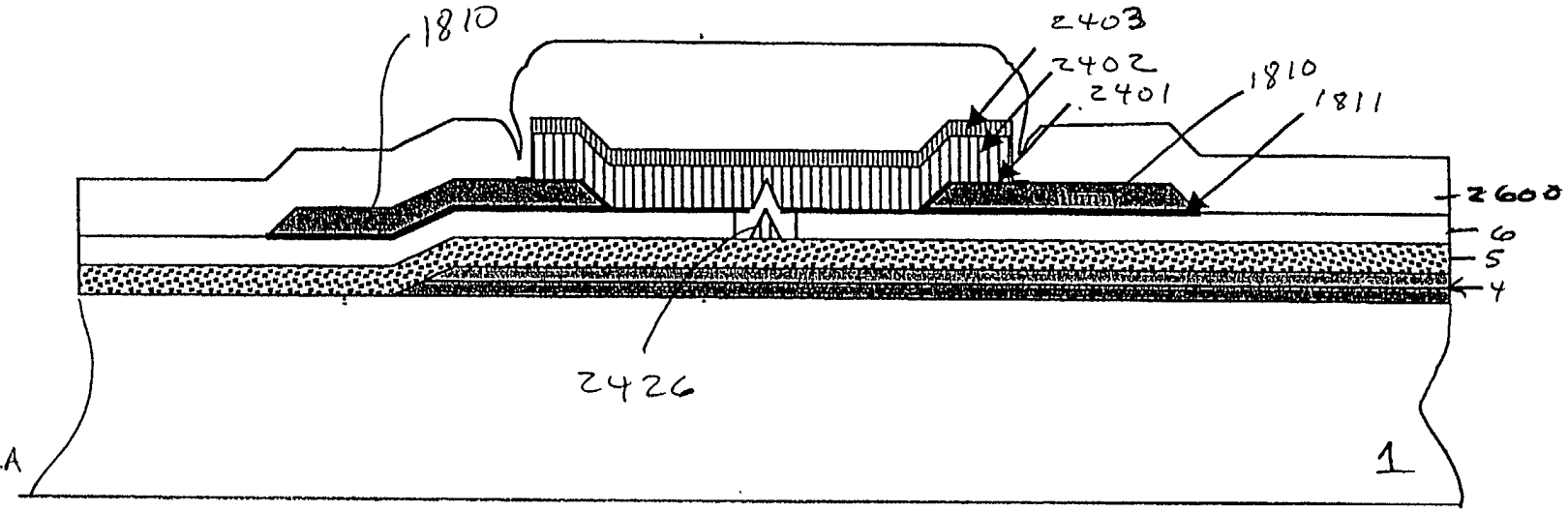


FIG. 26A

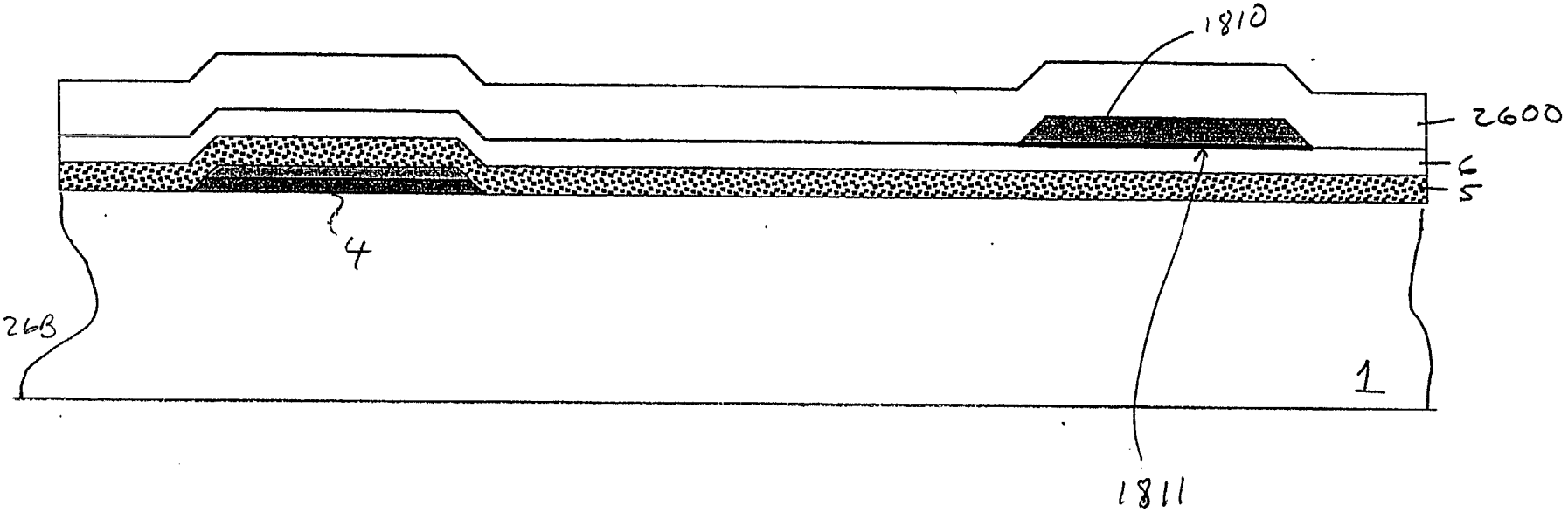


FIG. 26B

FIG 26C

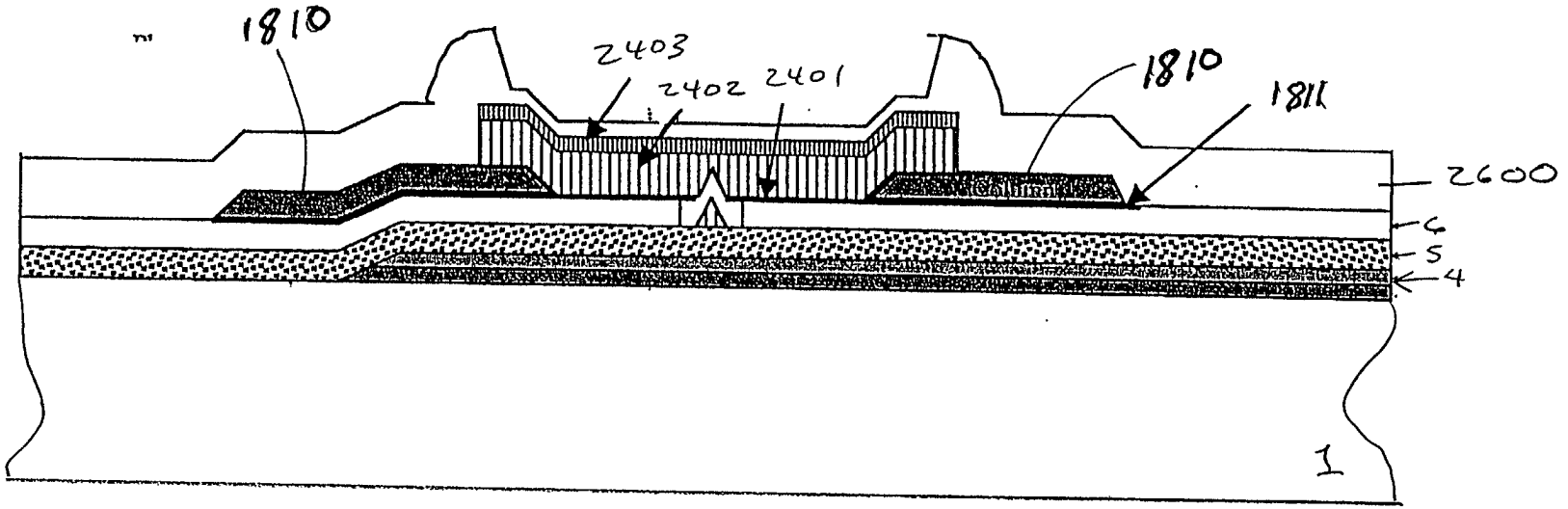


FIG 26D

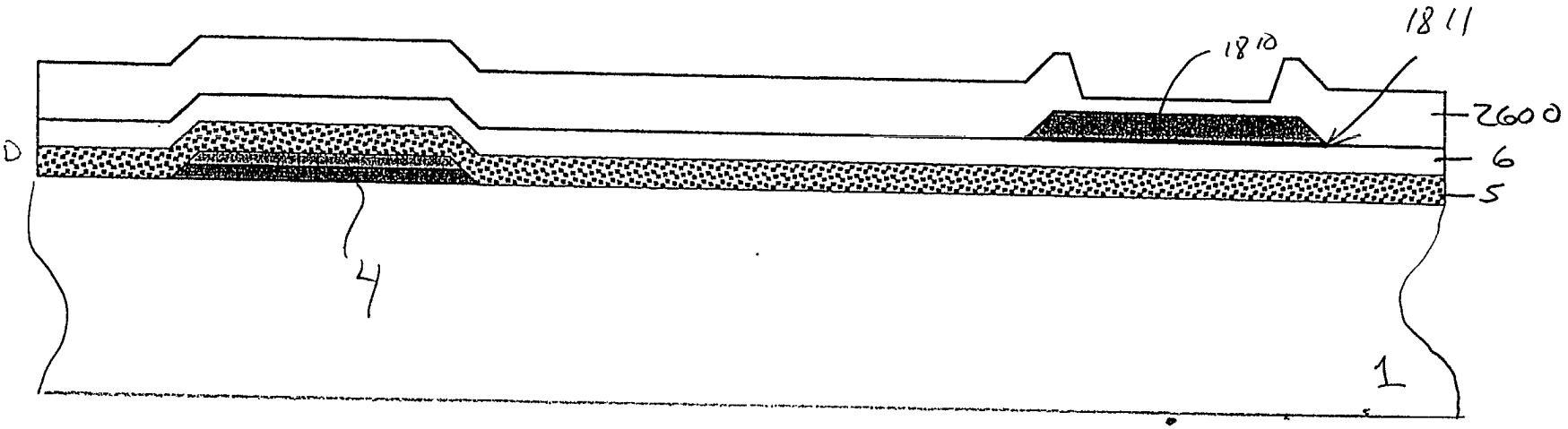


FIG 26E

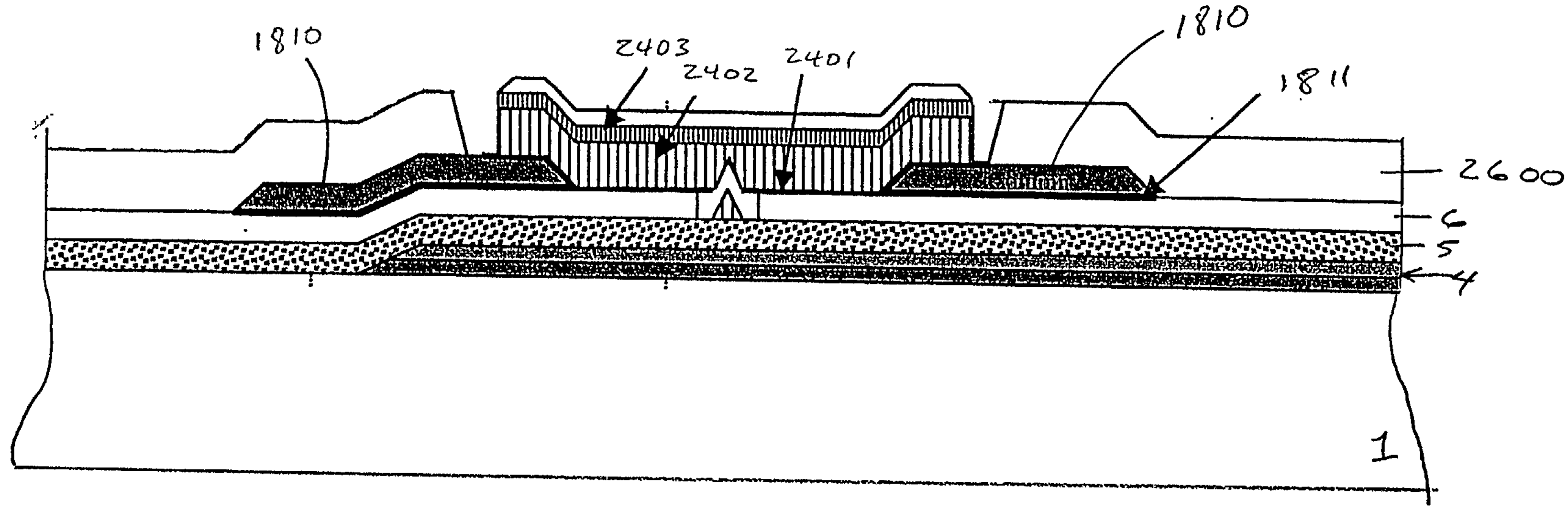


FIG 26F

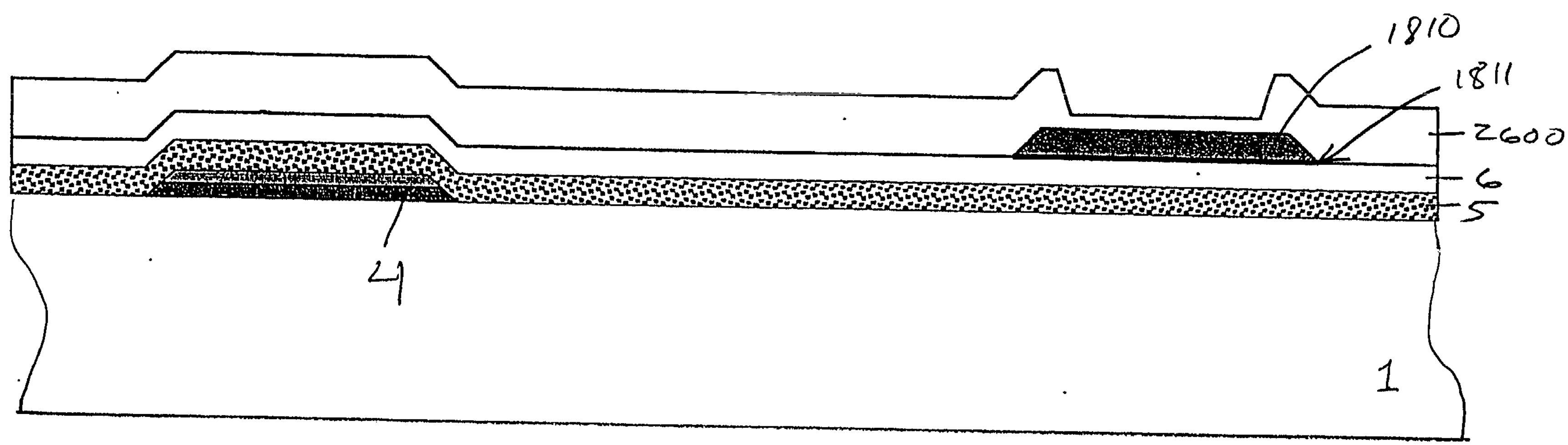


FIG 26G

FIG 26H

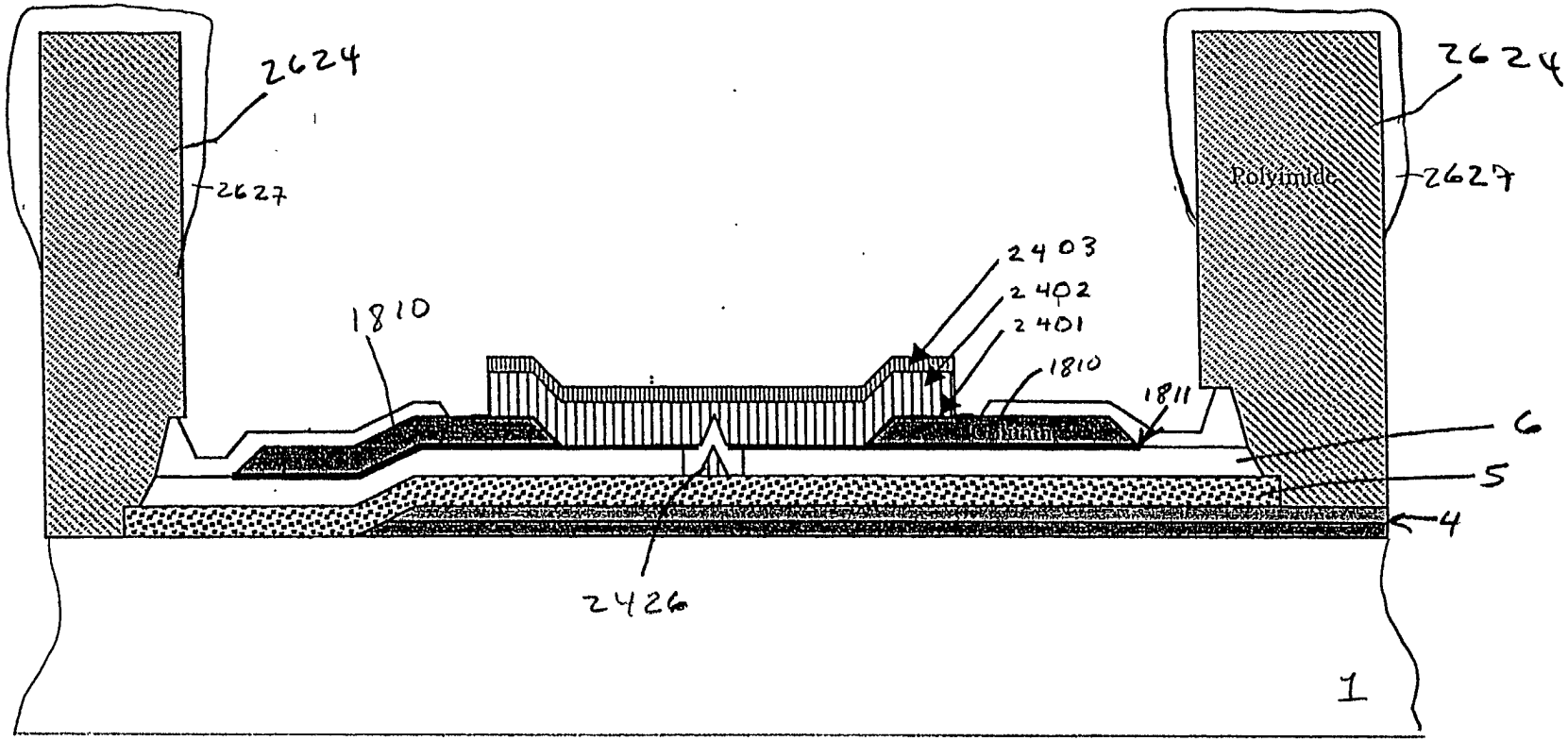


FIG 26 I

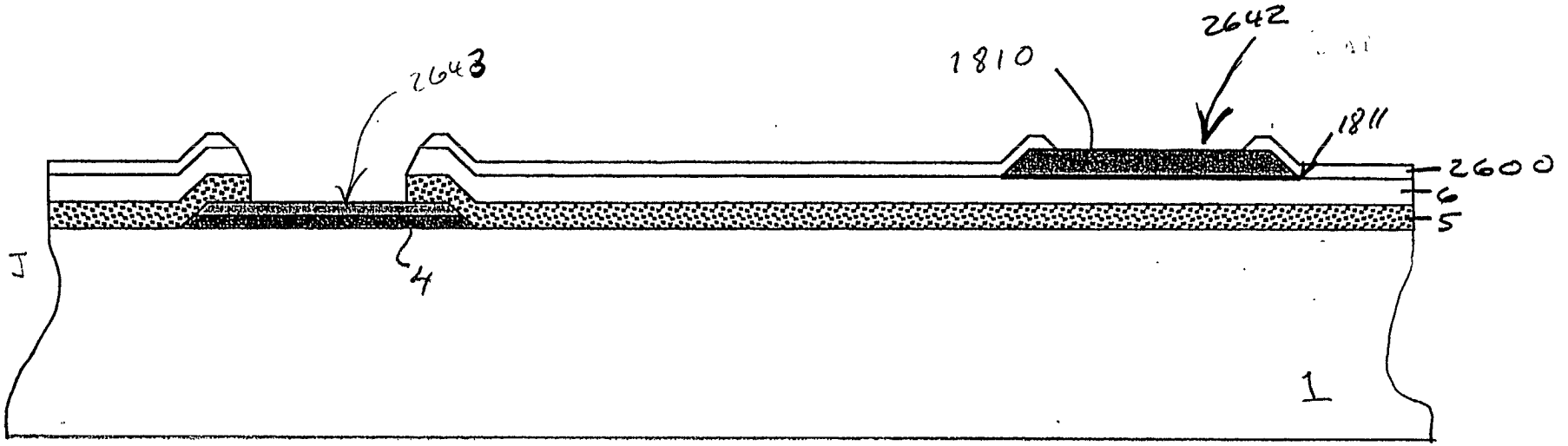


FIG 26 J

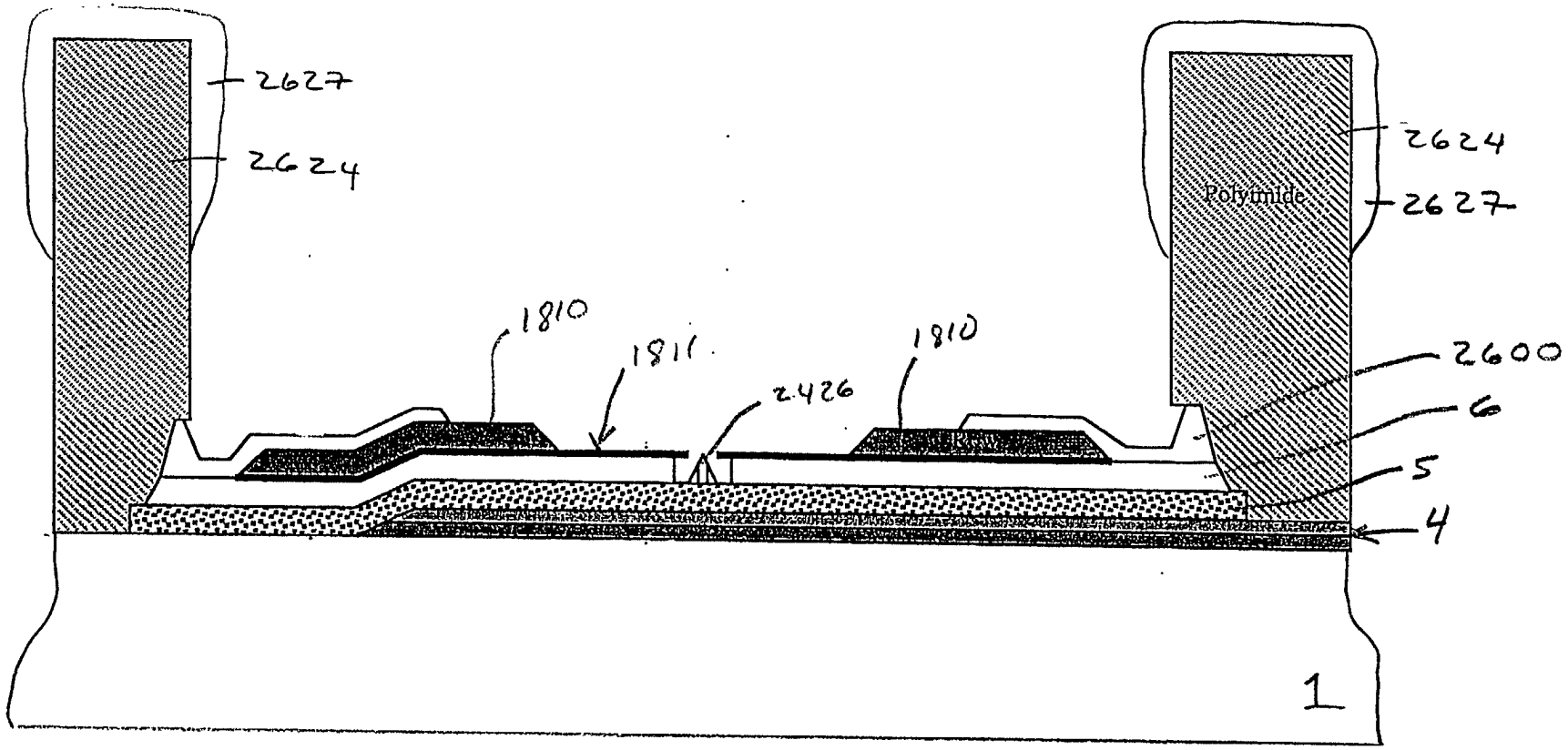


FIG 26K

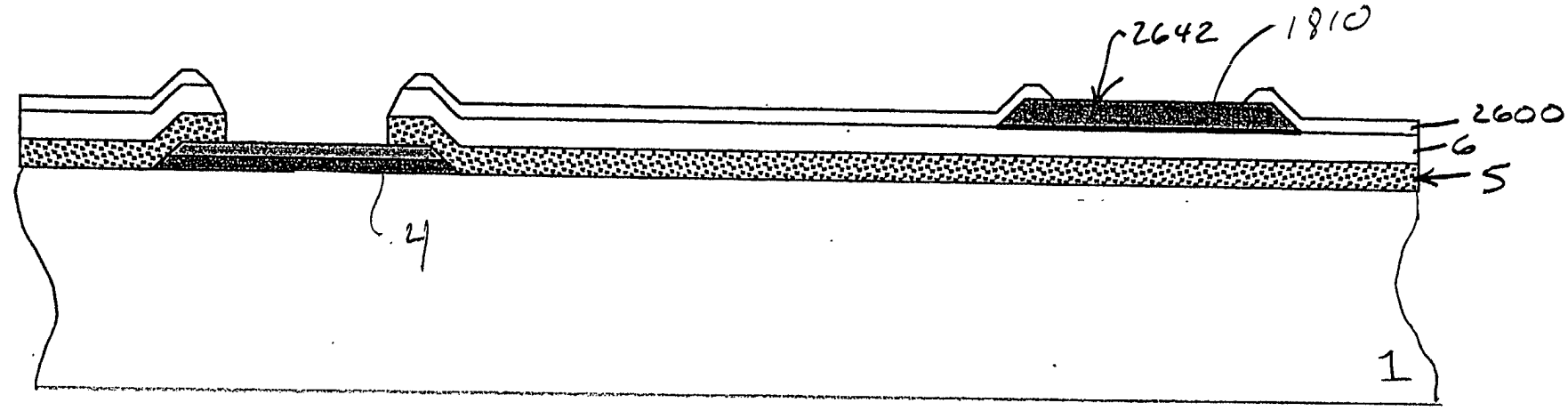


FIG 26L

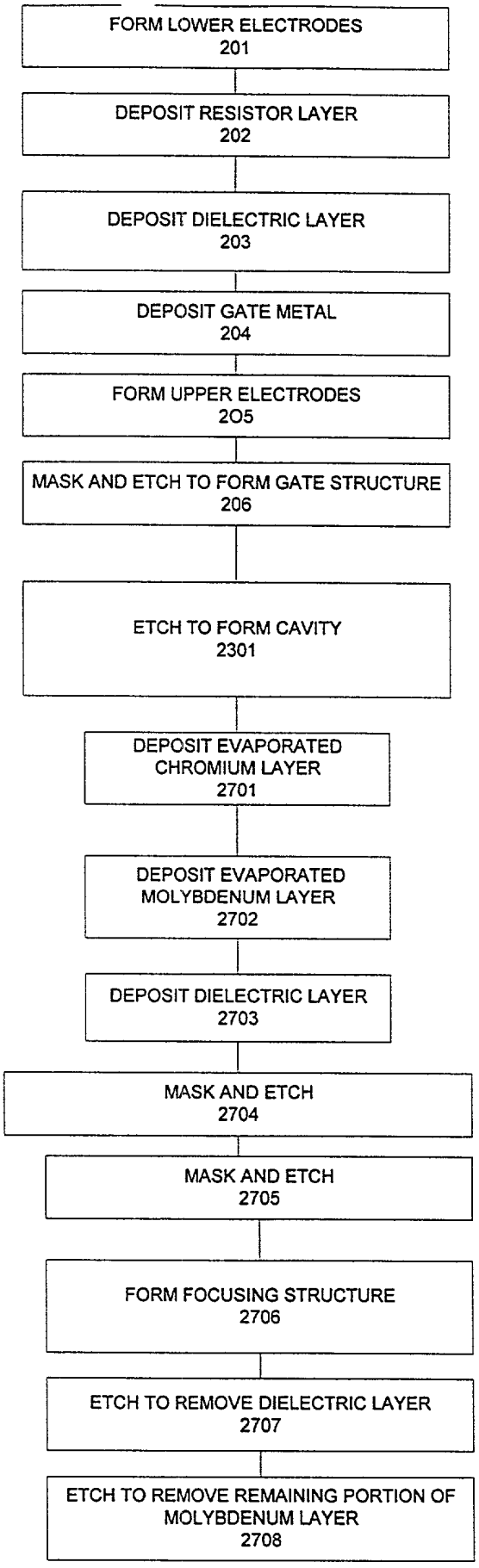

FORM LOWER ELECTRODES
201
DEPOSIT RESISTOR LAYER
202
DEPOSIT DIELECTRIC LAYER
203
DEPOSIT GATE METAL
204
FORM UPPER ELECTRODES
2O5
MASK AND ETCH TO FORM GATE STRUCTURE
206
ETCH TO FORM CAVITY
2301
DEPOSIT EVAPORATED
CHROMIUM LAYER
2701
DEPOSIT EVAPORATED
MOLYBDENUM LAYER
2702
DEPOSIT DIELECTRIC LAYER
2703
MASK AND ETCH
2704
MASK AND ETCH
2705
FORM FOCUSING STRUCTURE
2706
ETCH TO REMOVE DIELECTRIC LAYER
2707
ETCH TO REMOVE REMAINING PORTION OF
MOLYBDENUM LAYER
2708

FIG. 27

FIG 28A

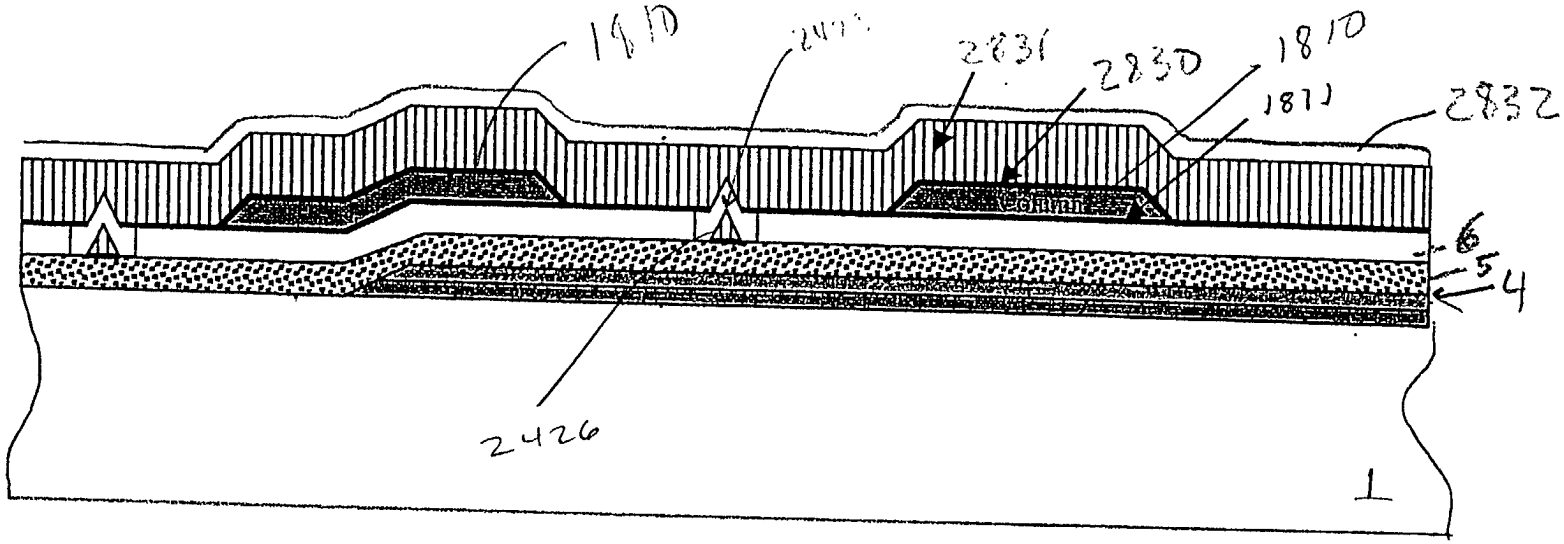
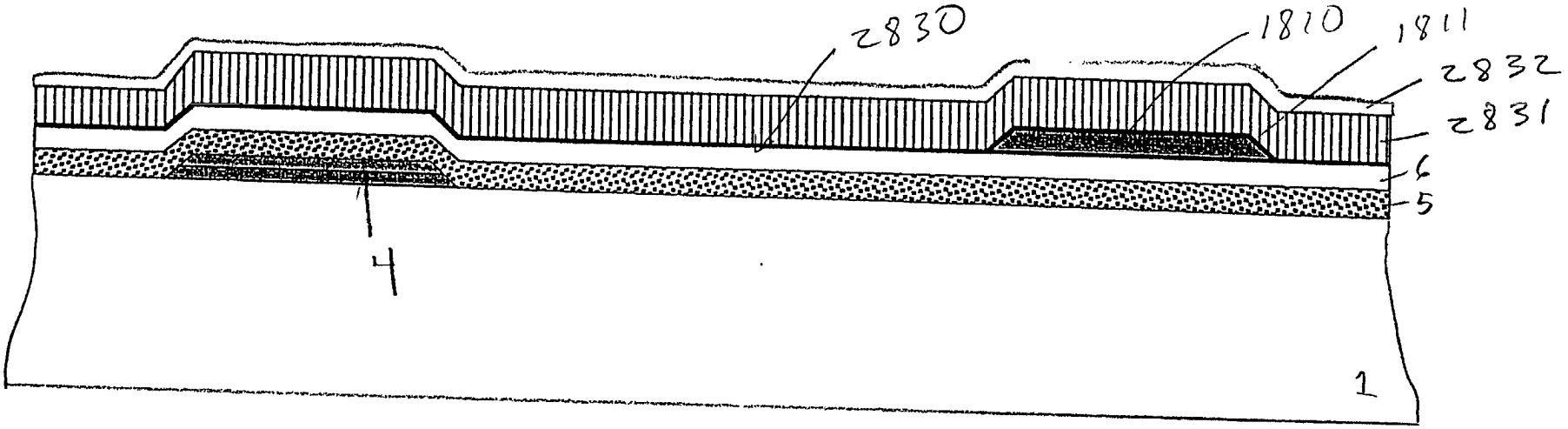


FIG 28B



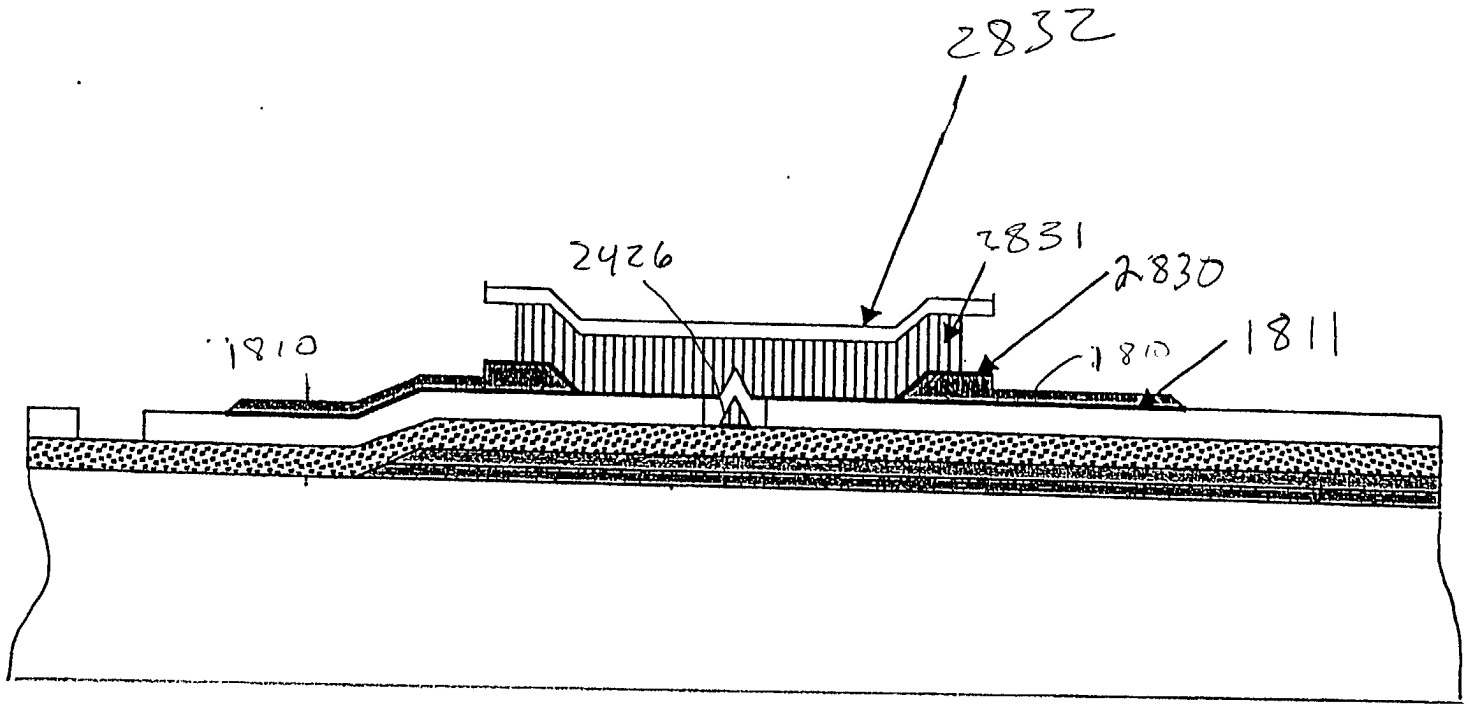


FIG 28 C

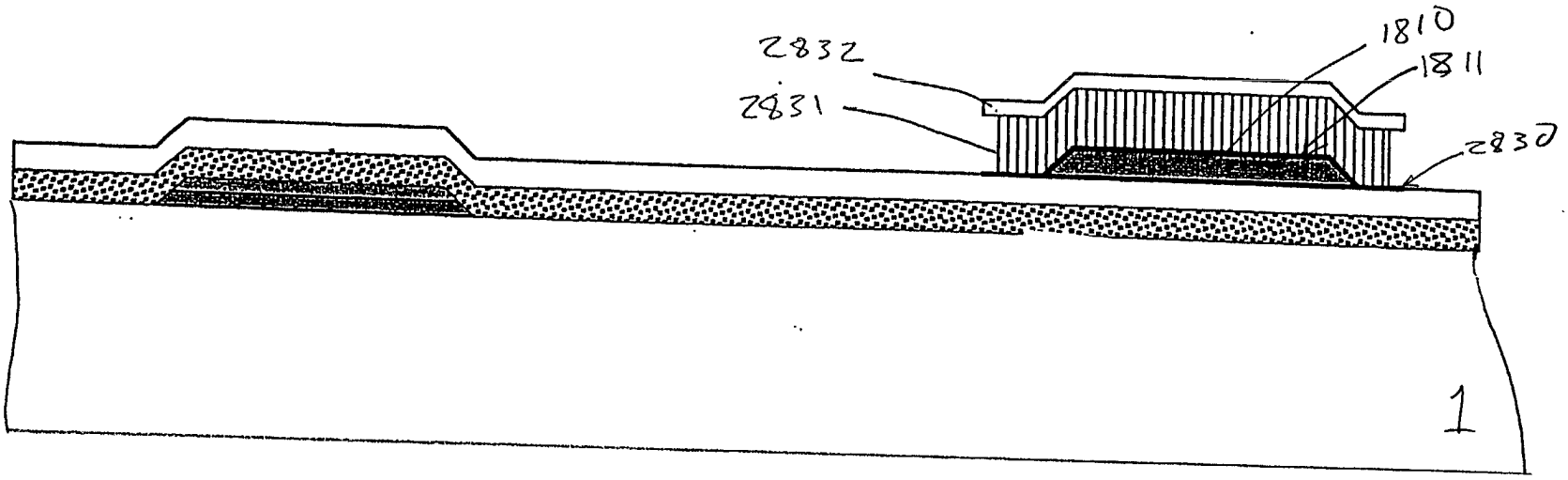


FIG 28 D

FIG 28E

FIG 28F

FIG 28G

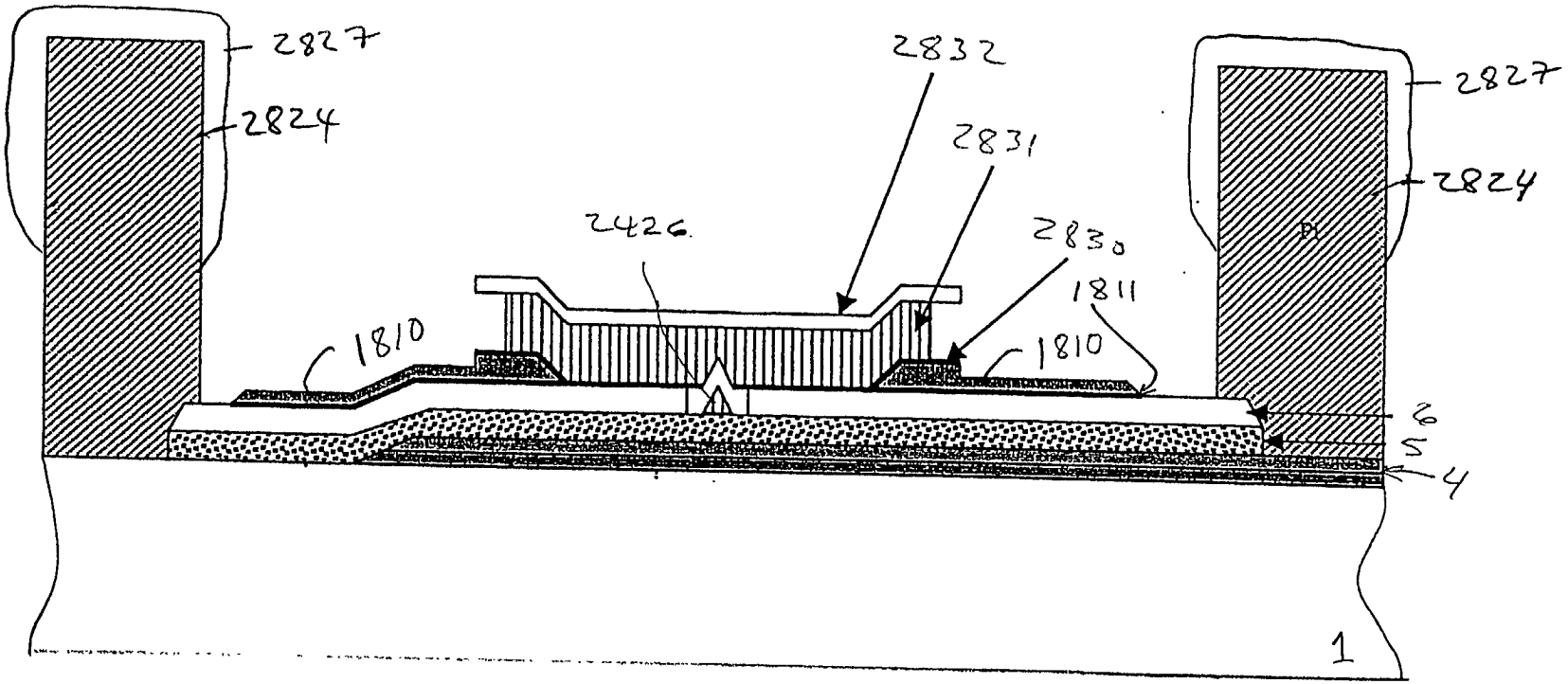


FIG 28H

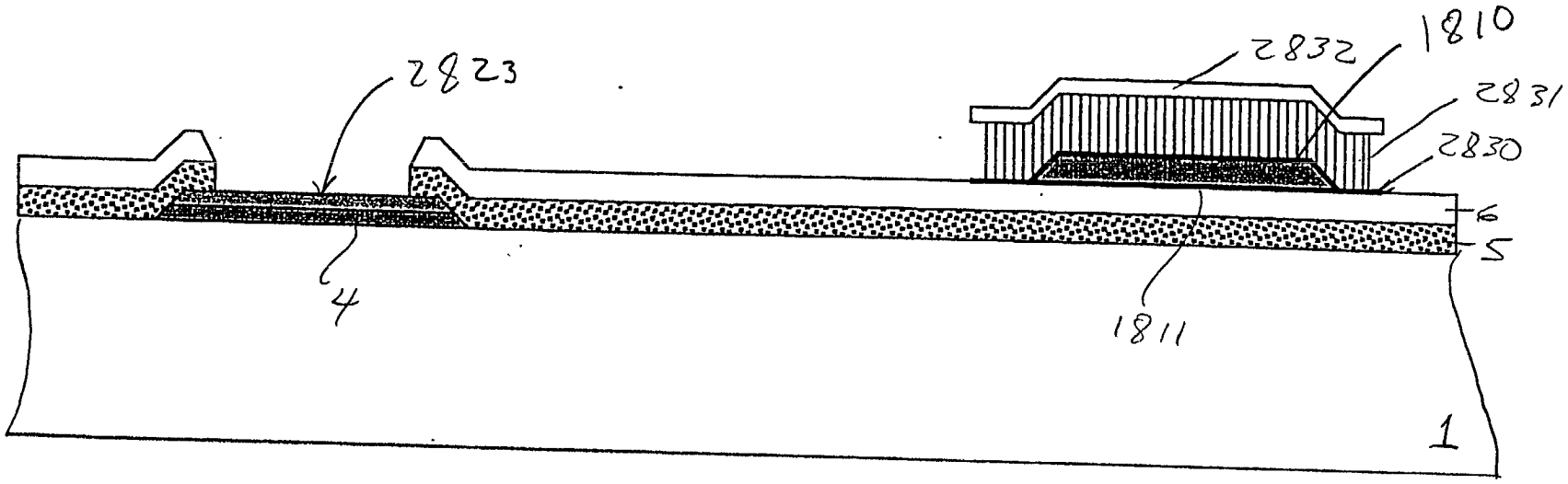


Fig 22 I

Fig 22 J

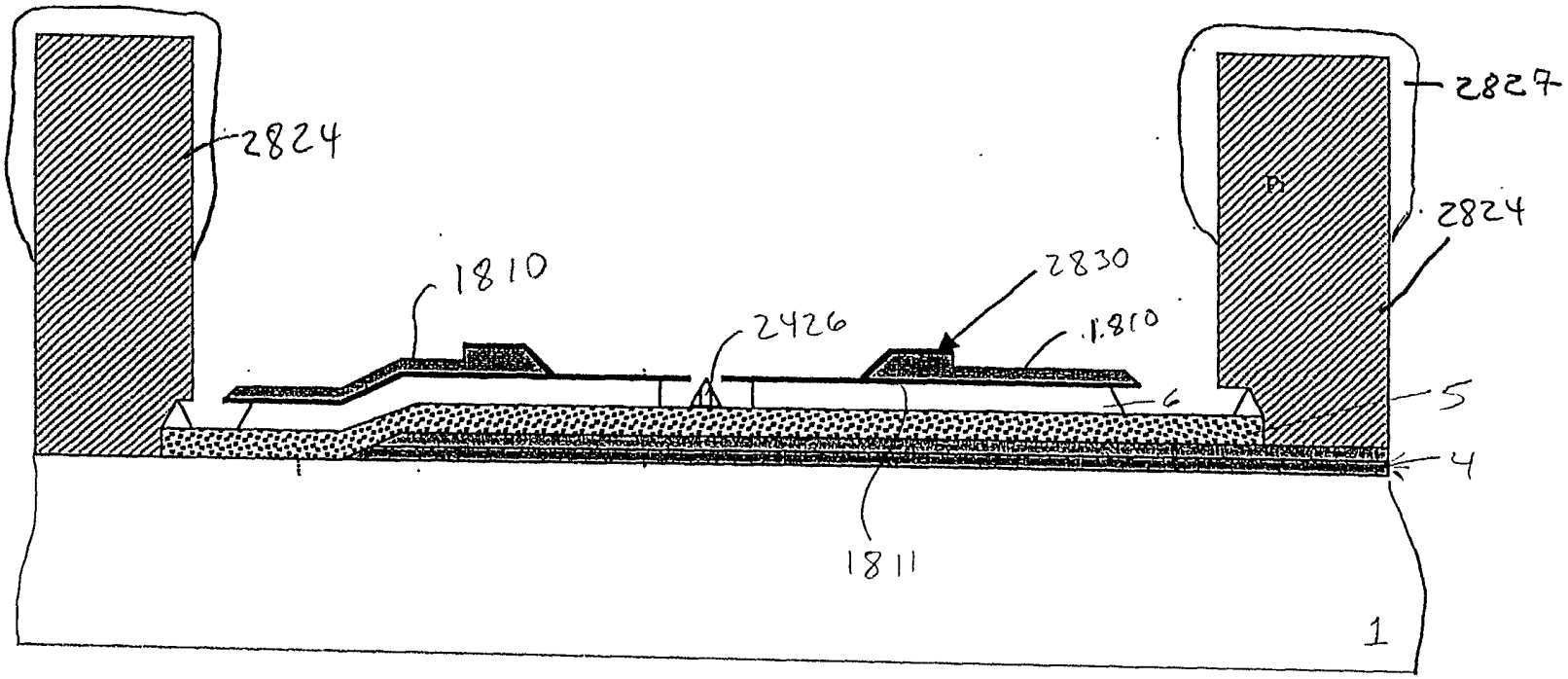


FIG 28K

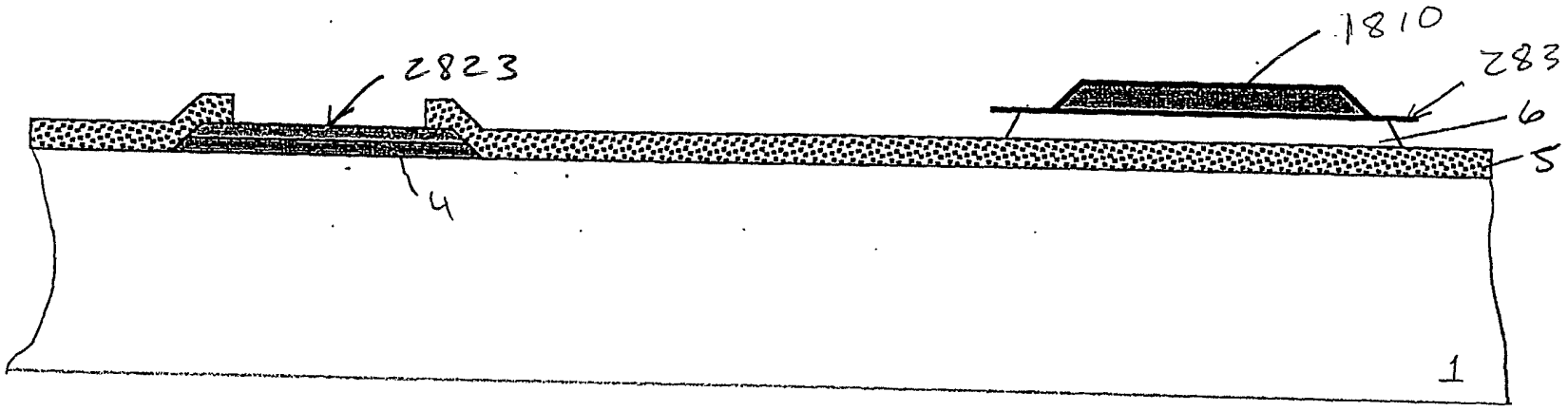


FIG 28L

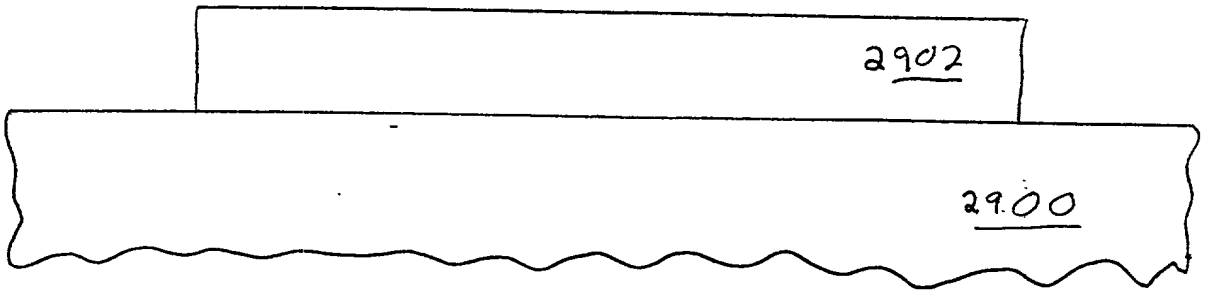


Fig. 29A

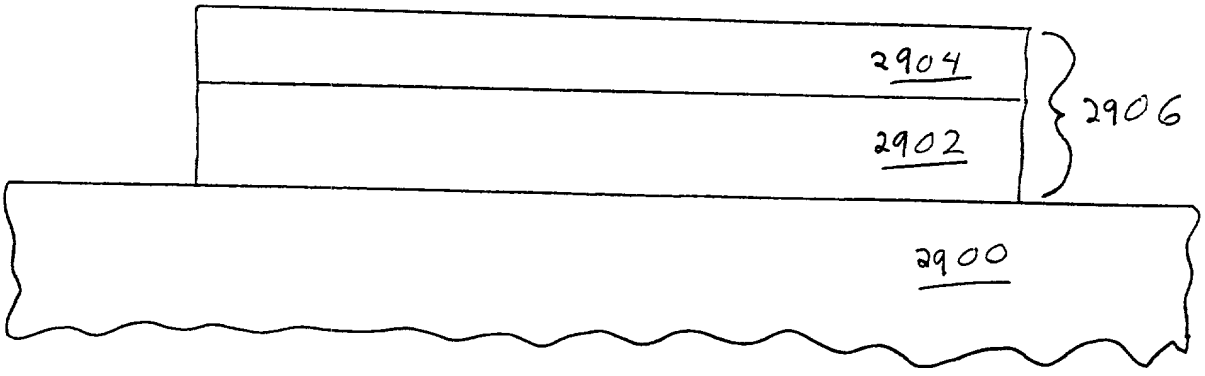


Fig. 29B

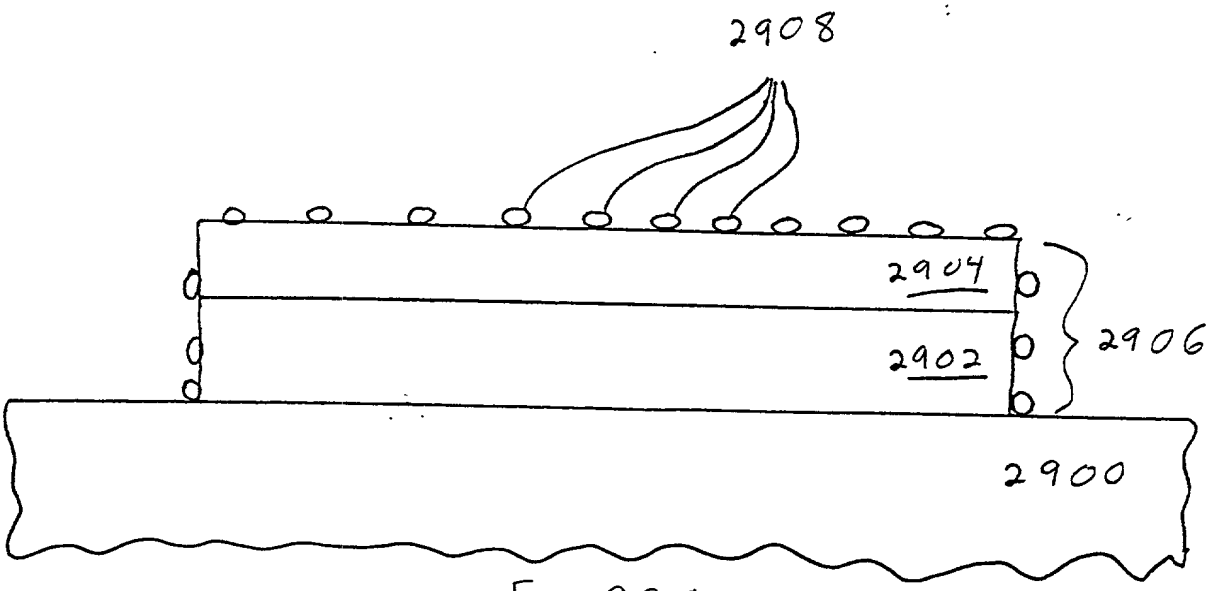


Fig. 29C

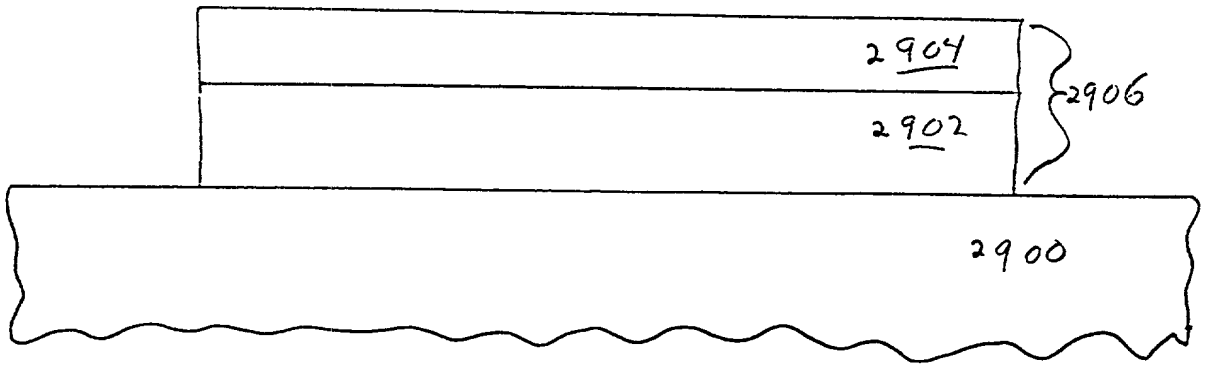


Fig. 29D

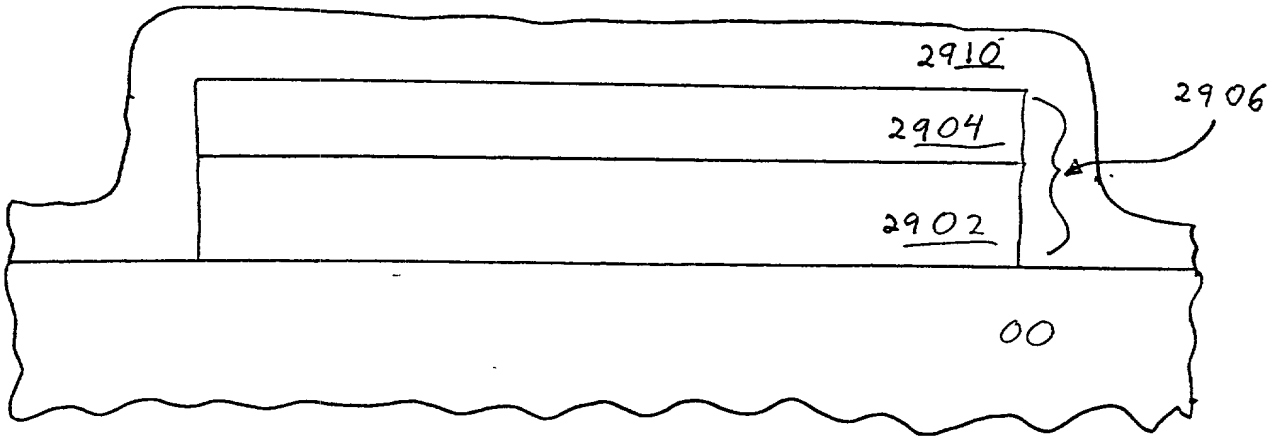


Fig. 29E

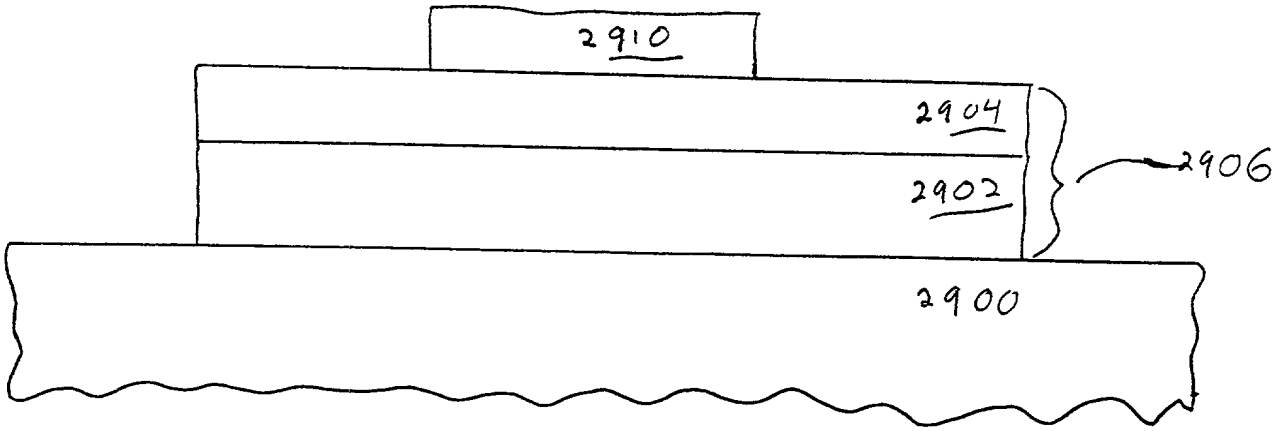


Fig. 29F

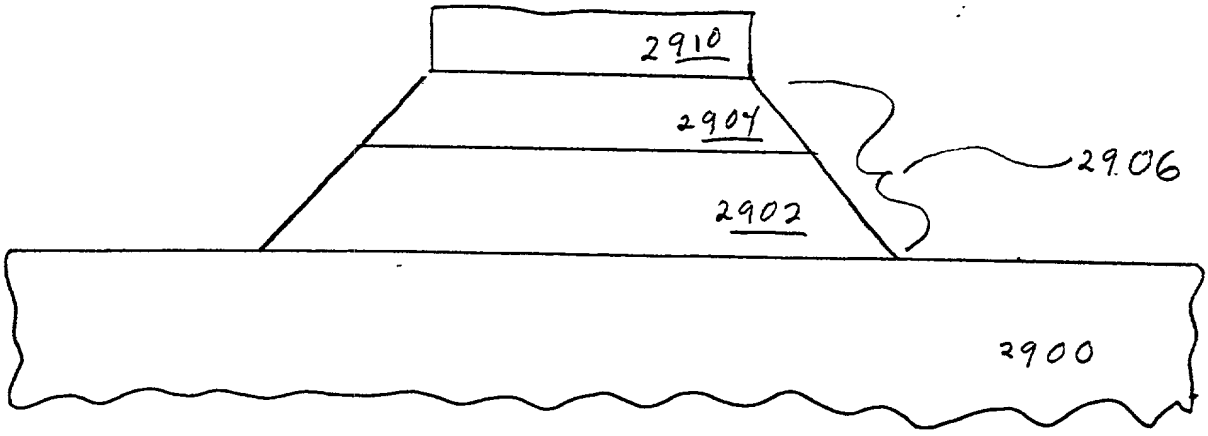


Fig. 29G

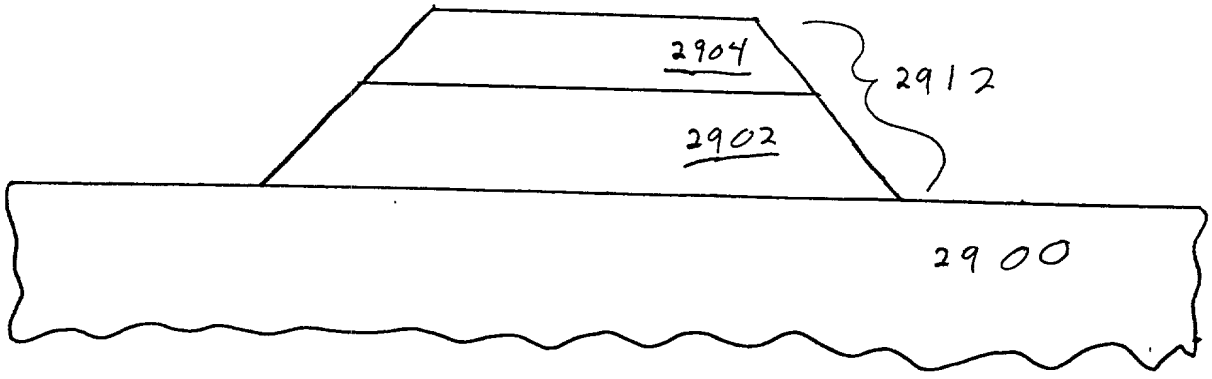


Fig. 29H

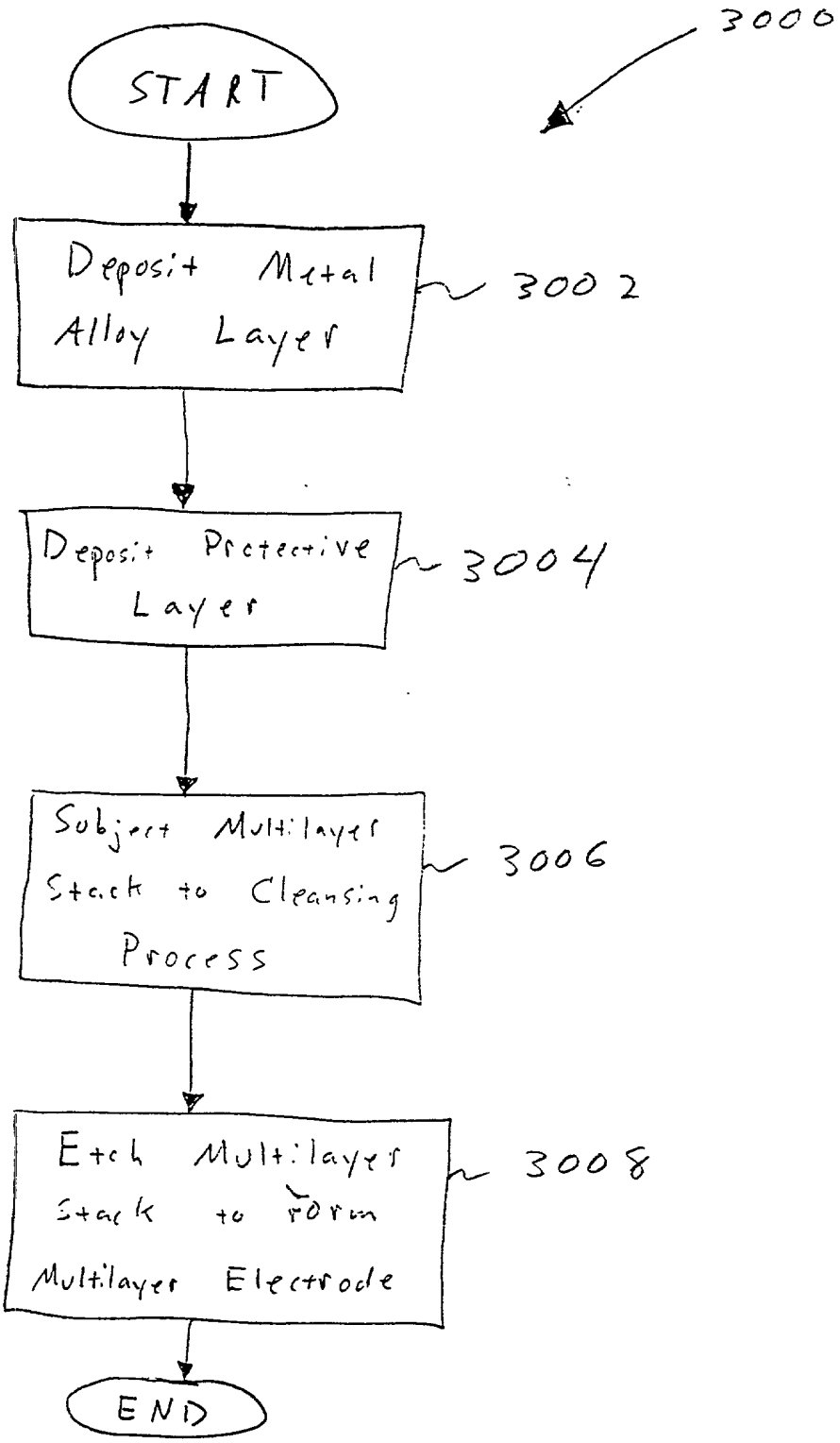

3000
START
Deposit Metal Alloy Layer
3002
Deposit Protective Layer
3004
Subject Multilayer Stack to Cleansing Process
3006
Etch Multilayer Stack to form Multilayer Electrode
3008
END

Fig. 30

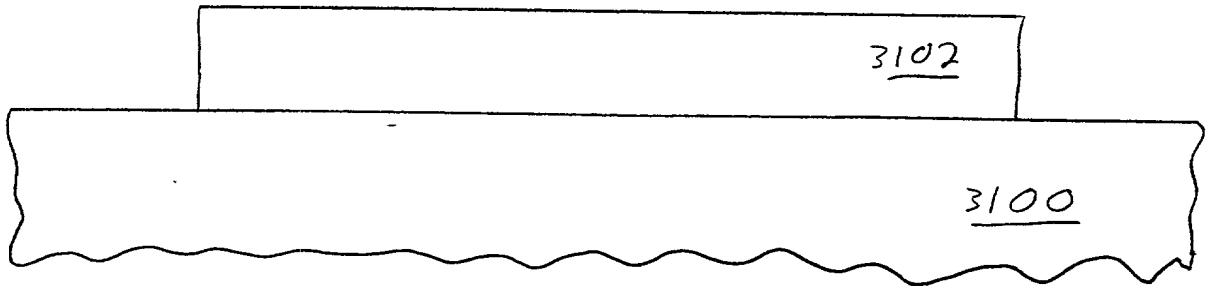


Fig. 31A

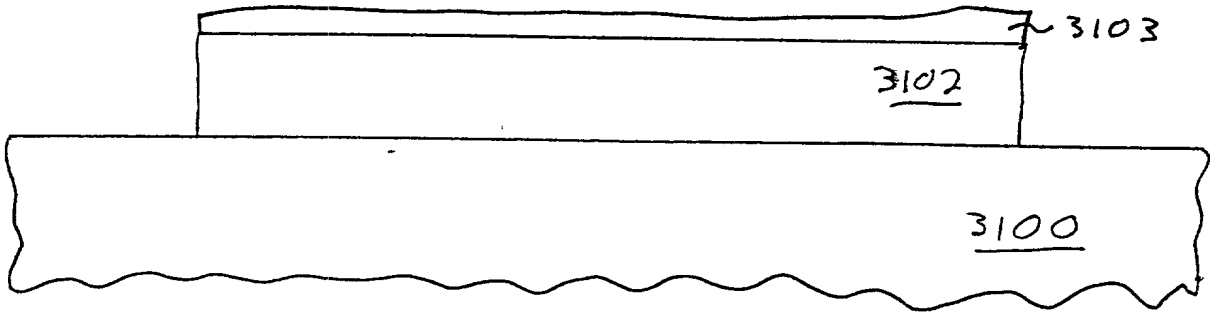


Fig. 31B

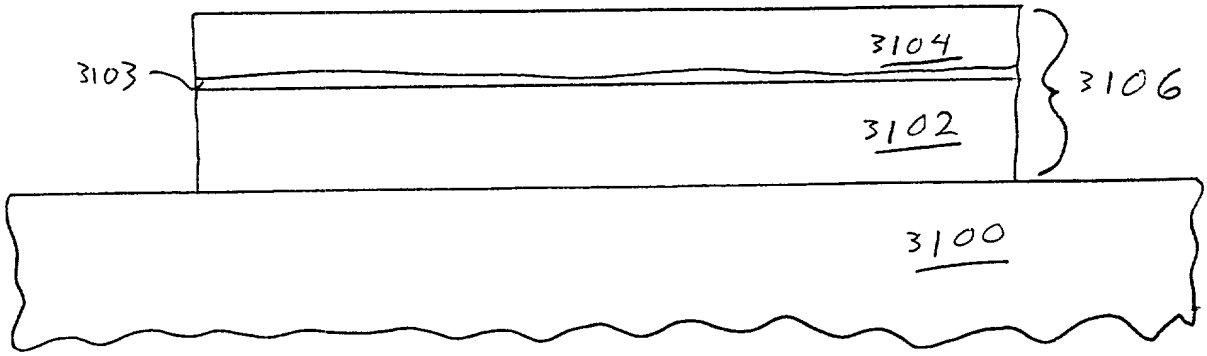


Fig 31C

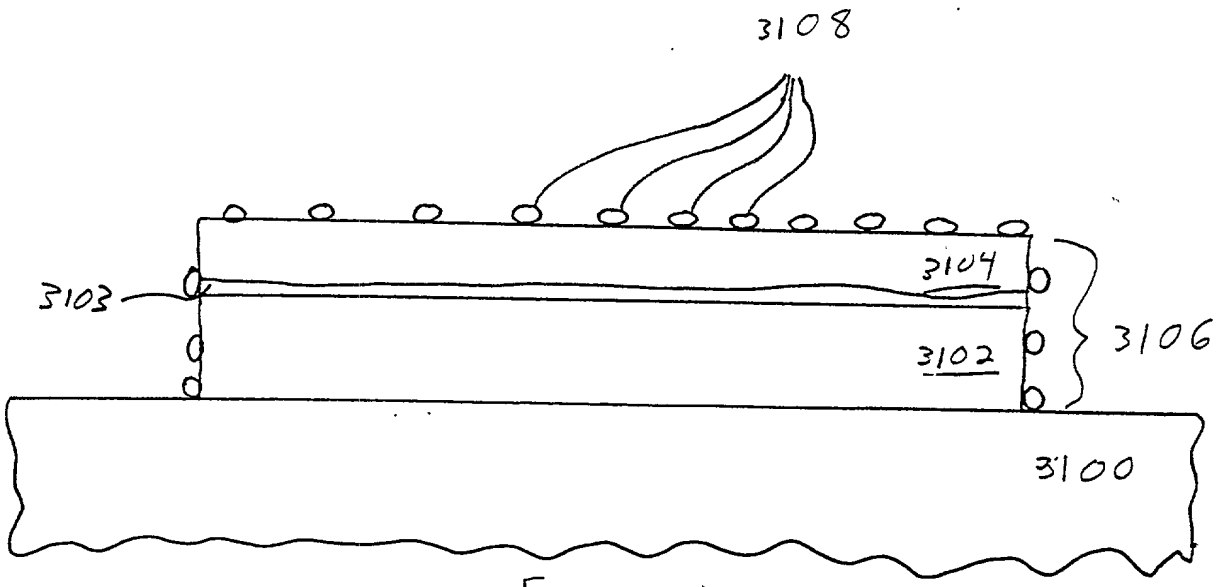


Fig. 31D

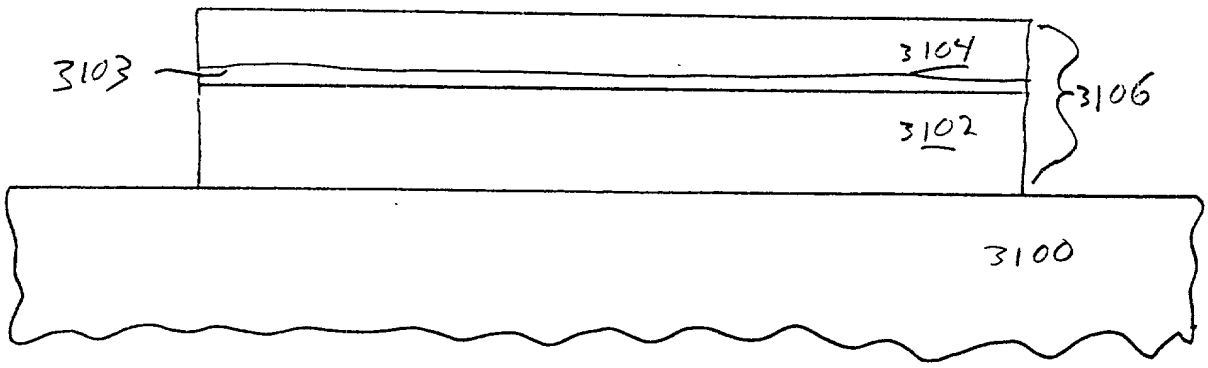


Fig. 31E

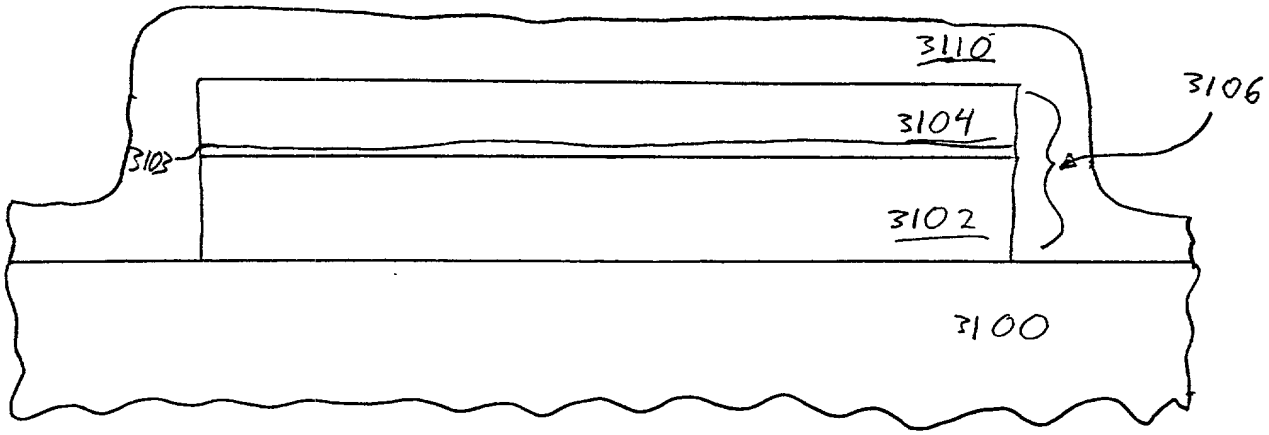


Fig. 31. F

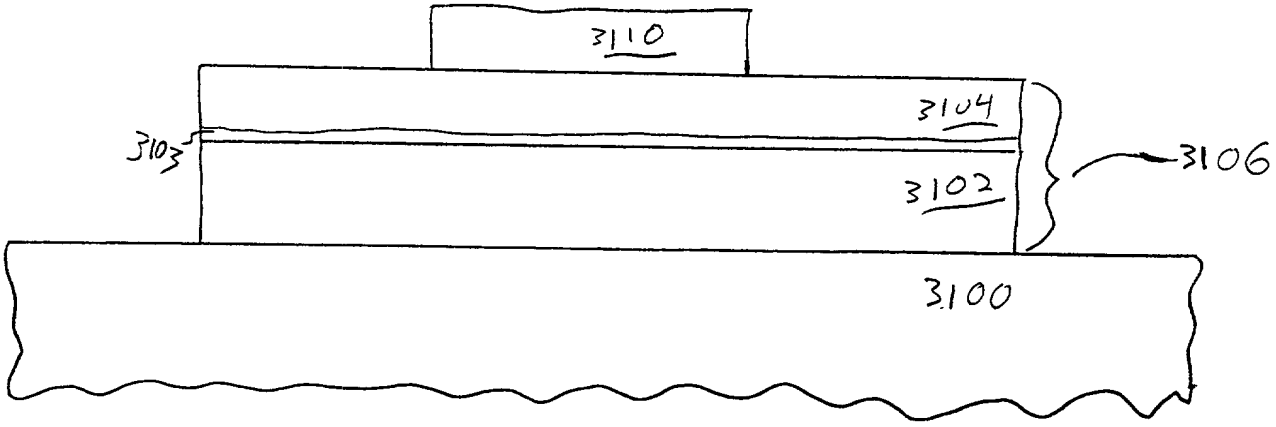


Fig. 31G

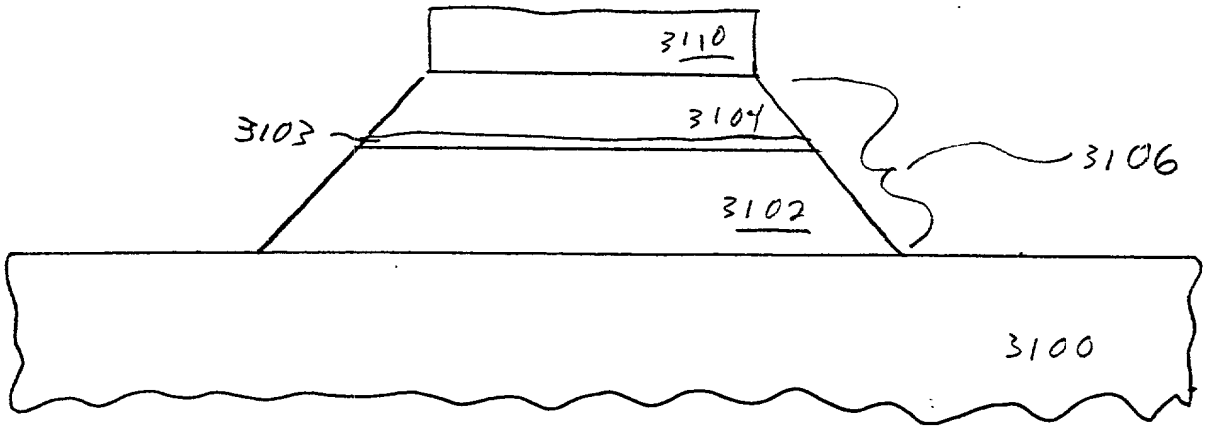


Fig. 31H

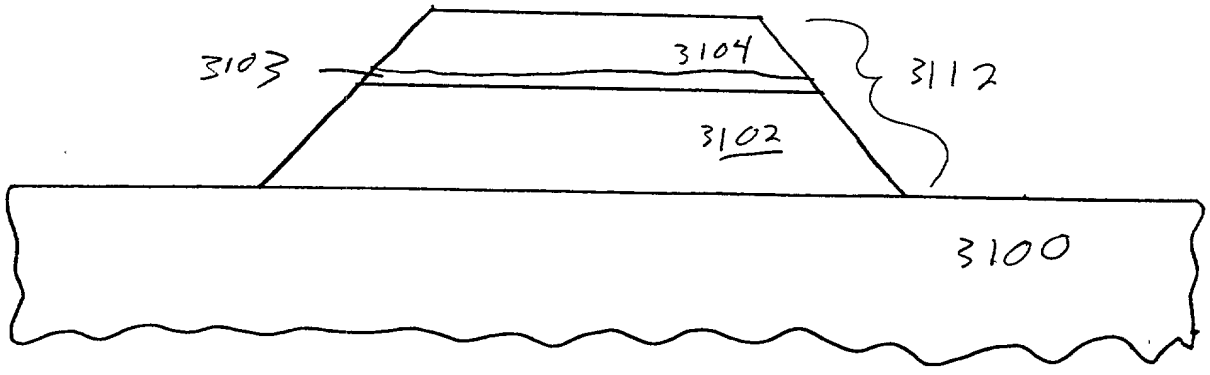


Fig. 31I

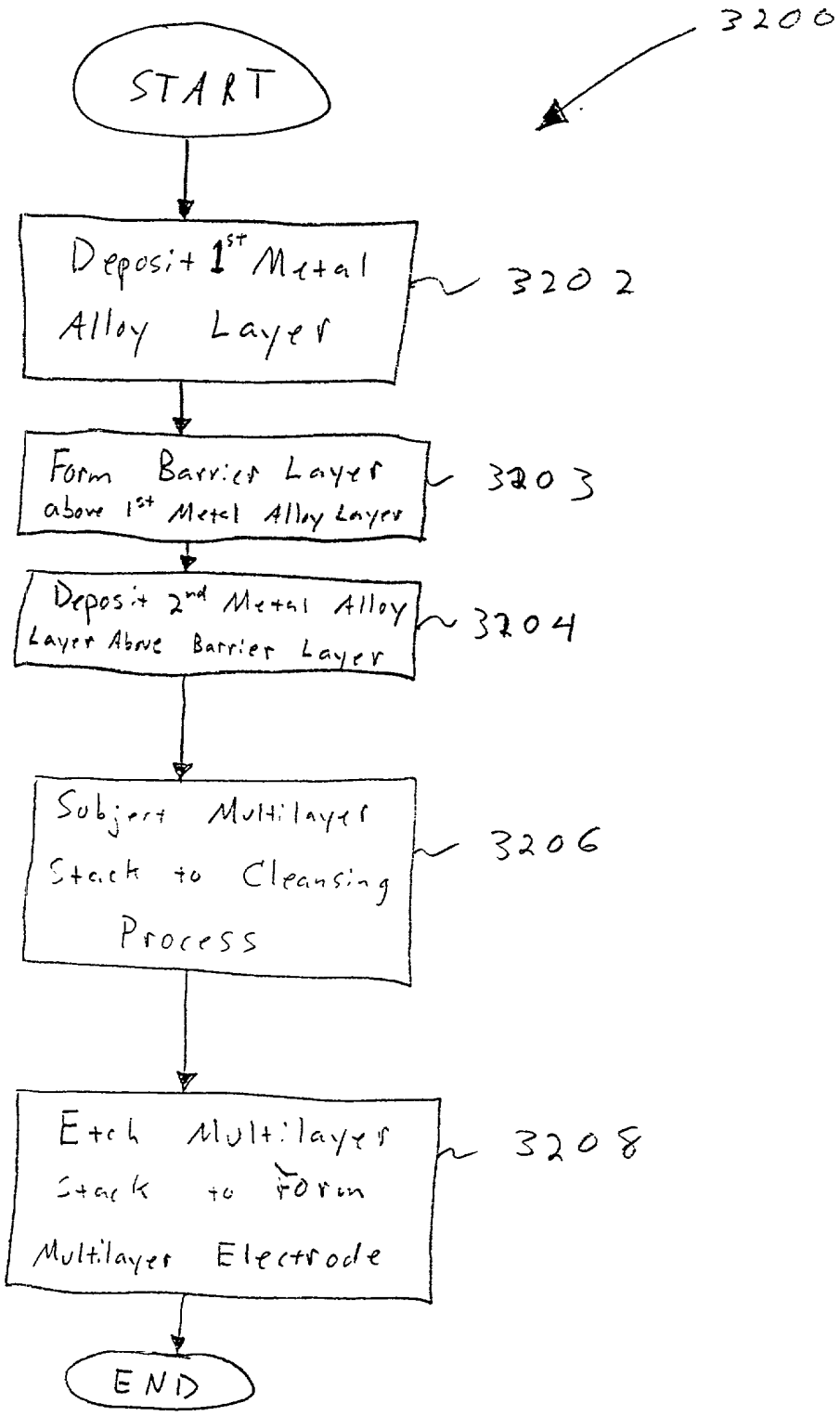

3200
START
Deposit 1st Metal Alloy Layer
3202
Form Barrier Layer above 1st Metal Alloy Layer
3203
Deposit 2nd Metal Alloy Layer Above Barrier Layer
3204
Subject Multilayer Stack to Cleansing Process
3206
Etch Multilayer Stack to Form Multilayer Electrode
3208
END

Fig. 32

Declaration and Power of Attorney for a Patent Application

Declaration

As below named inventor, I hereby declare that my residence post office address, and citizenship are as stated below my name. Further, I hereby declare that I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

MULTILAYER ELECTRODE STRUCTURE AND METHOD FOR FORMING MULTILAYER ELECTRODE STRUCTURE FOR A FLAT PANEL DISPLAY DEVICE

the specification of which:

X is attached hereto, or
____ was filed on ____ as application serial no. ____ : and
____ was amended on ____

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above; and

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

Foreign Priority Claim

I hereby claim foreign priority benefits under Title 35, United States Code Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Number	Country	Date Filed	Priority Claimed	
			yes	no
			yes	no

U.S. Priority Claim

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Serial Number	Filing Date	Status (patented/pending/abandoned)
09/421,781	10/19/99	pending

Power of Attorney

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent Trademark Office connected therewith.

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Anthony C. Murabito	Registration No.: 35,295
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Thomas M. Catale	Registration No.: P-46,434
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Kenneth N. Glass	Registration No.: 42,587
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Signatures

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor: **Jueng Gil Lee**

Inventor's Signature _____ Date _____
Residence _____ Citizenship _____
(City State)
P.O. Address _____

Full Name of Second/Joint Inventor: **Christopher J. Spindt**

Inventor's Signature _____ Date _____
Residence _____ Citizenship _____
(City State)
P.O. Address _____

Full Name of Third/Joint Inventor: **Johan Knall**

Inventor's Signature _____ Date _____
Residence _____ Citizenship _____
(City State)
P.O. Address _____

Full Name of Fourth/Joint Inventor: **Matthew A. Bonn**

Inventor's Signature _____ Date _____
Residence _____ Citizenship _____
(City State)
P.O. Address _____

Full Name of Fifth/Joint Inventor: **Kishore K. Chakravorty**

Inventor's Signature _____ Date _____
Residence _____ Citizenship _____
(City State)
P.O. Address _____